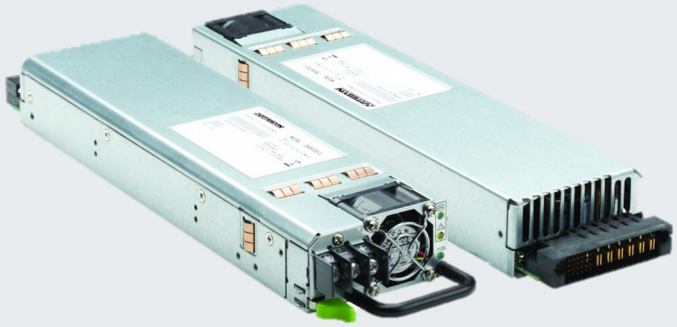
TECHNICAL REFERENCE NOTE

ARTESYN DS450DC-3 SERIES

450 Watts Distributed Power System



PRODUCT DESCRIPTION

Advanced Energy's Artesyn DS450DC series bulk front end power supplies are the DC-input versions of their DS450 AC-input counterparts. Mechanically identical to the AC versions, these products allow system operation from a Telco style 48Vdc input. Rated at 450 watts, the DS450DC power supplies generate a main DC output of 12Vdc and a 3.3Vdc for powering standby circuitry. Standard features include active current sharing, internal ORing FETs and an EEPROM for storing service data to facilitate efficient field replacement. An I^2C communication interface is provided for the FRU EEPROM data.

AT A GLANCE

Total Power

450 Watts

Input Voltage

36 to 75 Vdc

of Outputs

Single Main

SPECIAL FEATURES

- 1U x 2U form factor
- No minimum load required
- Internal ORing FETs
- Active power factor correction
- 8.4W/in^3 (DS450)
- Internal fan speed control
- Inrush current control
- Full digital control
- N+1 redundant
- Hot plug operation
- Active current sharing
- Built-in cooling fan (40mm x 28mm)
- I^2C communication interface bus
- EEPROM for FRU data
- Amber LED status, Fan_Fail
- Green LED status, Power Good / DC_OK Status (VIN_GOOD)
- Fan fail tach output signal
- One year warranty

SAFETY

- UL/cUL62368 (UL Recognized)
- NEMKO + CB Report EN62368
- EN62368
- CE Mark
- China CCC
- UKCA Mark

TYPICAL APPLICATIONS

- Industrial

PMBus® Power Management. Defined.

RoHS

MODEL NUMBERS

Standard	Output Voltage	Minimum Load	Maximum Load	Stand-By Supply	Air Flow Direction
DS450DC-3	12.0Vdc	0A	37.0A	3.3V @ 3.0A	Normal (DC Connector to Handle)
DS450DC-3-002	12.0Vdc	0A	37.0A	3.3V @ 3.0A	Reversed (Handle to DC Connector)
DS450DC-3-401	12.0Vdc	0A	37.0A	3.3V @ 3.0A	Normal (DC Connector to Handle)

Options

None

ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings

Stress in excess of those listed in the "Absolute Maximum Ratings" may cause permanent damage to the power supply. These are stress ratings only and functional operation of the unit is not implied at these or any other conditions above those given in the operational sections of this TRN. Exposure to any absolute maximum rated condition for extended periods may adversely affect the power supply's reliability.

Table 1. Absolute Maximum Ratings

Parameter	Models	Symbol	Min	Typ	Max	Unit
Input Voltage						
DC continuous operation	All models	$V_{IN,DC}$	36	-	75	Vdc
Maximum Output Power (Main + Stand-by)	All models	$P_{O,max}$	-	-	450	W
Isolation Voltage						
Input to outputs	All models		-	-	2200	Vdc
Input to safety ground	All models		-	-	2200	Vdc
Outputs to safety ground	All models		-	-	N/A	Vdc
Ambient Operating Temperature	All models	T_A	-10	-	50	^{O}C
Storage Temperature	All models	T_{STG}	-40	-	70	^{O}C
Humidity (non-condensing)						
Operating	All models		20	-	90	%
Non-operating	All models		-	-	95	%
Altitude						
Operating	All models		-	-	10000	Feet
Non-operating	All models		-	-	35000	Feet

ELECTRICAL SPECIFICATIONS

Input Specifications

Table 2. Input Specifications

Parameter	Condition	Symbol	Min	Typ	Max	Unit
Operating Input Voltage, DC	All	V_{DC}	36	48	75	Vdc
Maximum Input Current ($I_O = I_{O,max}$, $I_{SB} = I_{SB,Max}$)	$V_{IN,DC} = 40V_{DC}$	$I_{IN,max}$	-	-	16	A
Standby Input Current (V_O Off, I_{SB} = 0A)	$V_{IN,DC} = 36V_{DC}$ $V_{IN,DC} = 75V_{DC}$	$I_{IN,standby}$	- -	- -	600 300	mA
No Load Input Current (V_O On, I_O = 0A, I_{SB} = 0A)	$V_{IN,DC} = 36V_{DC}$ $V_{IN,DC} = 75V_{DC}$	I_{IN,no_load}	- -	- -	400 200	mA
Standby Input Power (V_O Off, I_{SB} = 0A)	All Modules	$W_{IN,standby}$	-	-	20	W
Startup Surge Current (Inrush) @ 25°C	$V_{IN,DC} = 75V_{DC}$		-	-	21	A
Input Fuse	Internal, Blade, 19x20mm, 25A, 80V		-	-	25	A
Isolation - Input to Output			-	2200	-	Vdc
Isolation - Input to Chassis			-	2200	-	Vdc
DCDC Switching Frequency	All Modules	$f_{SW,DC-DC}$	125	-	145	KHz
Operating Efficiency @ 25°C	$I_O = I_{O,max}$ $V_{IN,DC} = 36V_{DC}$ $V_{IN,DC} = 75V_{DC}$	η	78 84	- -	- -	%
System Stability Phase Margin Gain Margin			 45 10	 - -	 - -	 ∅ dB

ELECTRICAL SPECIFICATIONS

Output Specifications

Table 3. Output Specifications

Parameter		Condition	Symbol	Min	Typ	Max	Unit
Output Regulation	All models	Inclusive of set-point, temperature change, warm-up drift and dynamic load	V_O	11.4	12.0	12.6	V
	DS450DC-3 DS450DC-3-002 DS450DC-3-401		V_{SB}	3.13	3.30	3.47	V
Output Ripple, pk-pk	All models	Measure with a 0.1µF ceramic capacitor in parallel with a 10µF tantalum capacitor, 0 to 20MHz bandwidth	V_O	-	-	120	mV_{PK-PK}
	DS450DC-3 DS450DC-3-002 DS450DC-3-401		V_{SB}	-	-	60	mV_{PK-PK}
Output Current	All models	All	I_O	0	-	37.0	A
	DS450DC-3 DS450DC-3-002 DS450DC-3-401		I_{SB}	0	-	3.0	A
V_O Current Share Accuracy		50% to 100% I_O 10% to 20% I_O		- -	- -	10 20	$\%I_O$
Minimum Current Sharing Loading				10	-	-	$\%I_{O,max}$
Main Output Load Capacitance		Start up	C_O	0	-	100	uF/A
Main Output Dynamic Response Peak Deviation Settling Time		25% load change Slew rate = 1A/us	$\pm\%V_O$ T_s	- -	- -	3 5	% mSec

ELECTRICAL SPECIFICATIONS

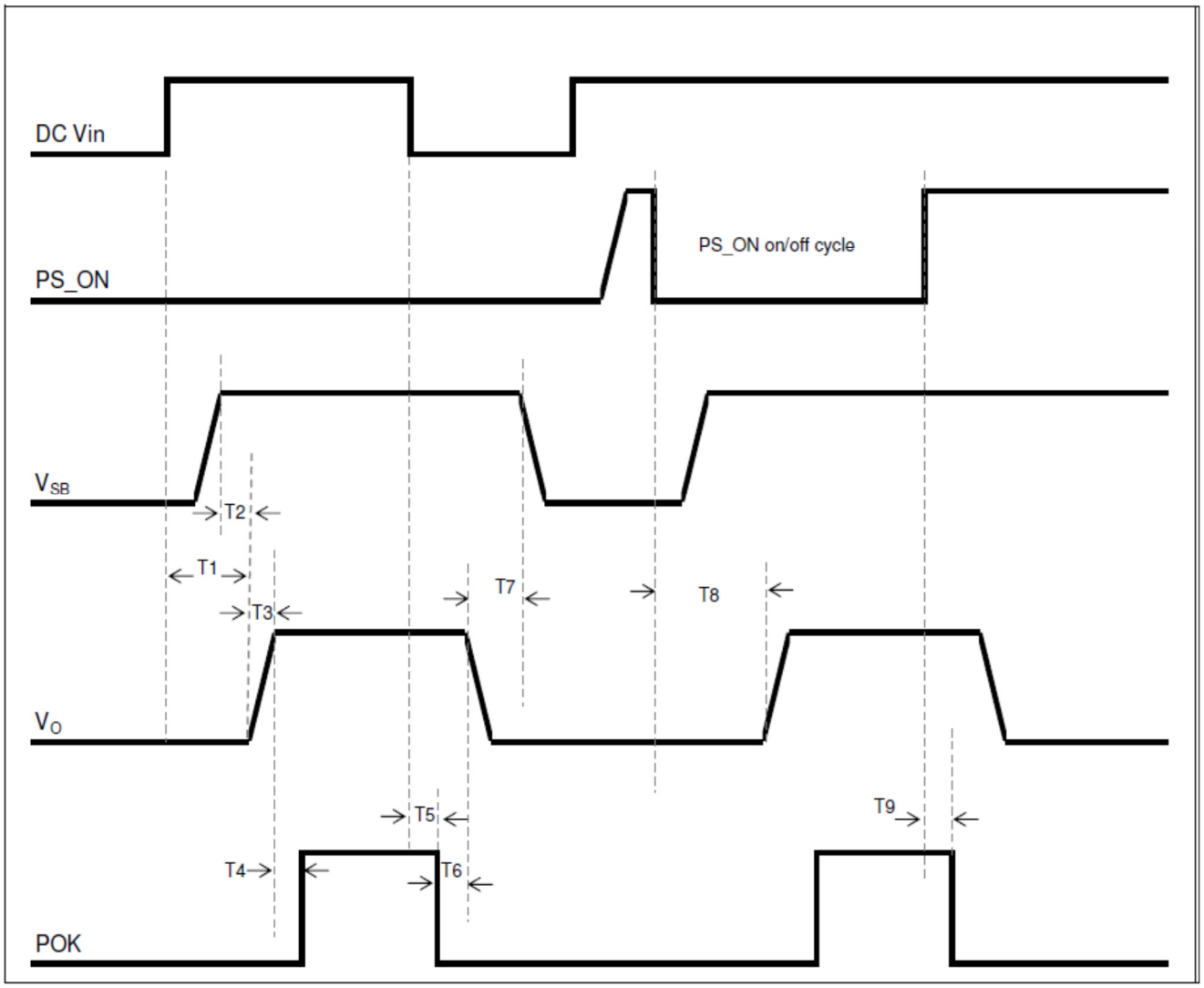
System Timing Specifications

Table 4. System Timing Specifications

Label	Parameter	Min	Typ	Max	Unit
T1	Delay from DC being applied to V_O being within regulation lower limit.	-	-	3000	mSec
T2	Delay from V_{SB} being within regulation upper limit to V_O being within lower regulation limit.	5	-	-	mSec
T3	V_O rise time, 0V to V_O in regulation.	3	-	300	mSec
T4	Delay from V_O output voltages within regulation limits to POK asserted high.	100	-	500	mSec
T5	Delay from loss of DC to de-assertion of POK.	1	-	-	mSec
T6	Delay from de-assertion of POK to output voltages within upper regulation limits.	0.1	-	10	mSec
T7	Delay from V_O out of regulation to V_{SB} output voltages within regulation limits.	5	-	-	mSec
T8	Delay from PS_ON active to V_O output voltages within lower regulation limits.	-	-	300	mSec
T9	Delay from PS_ON deactive to POK de-asserted low.	-	-	50	mSec

ELECTRICAL SPECIFICATIONS

System Timing Diagram



ELECTRICAL SPECIFICATIONS

DS450DC-3 Performance Curves

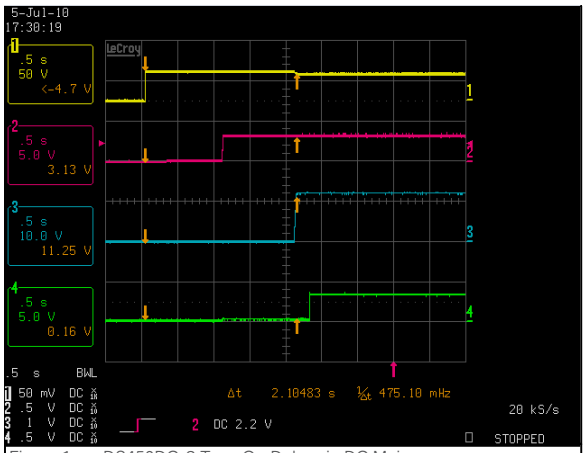


Figure 1: DS450DC-3 Turn-On Delay via DC Mains
Vin = 36Vdc Load: I_O = 37A I_{SB} = 3A (3.3V)
Ch 1: DC Mains Ch 2: V_{SB} Ch 3: V_O Ch 4: POK

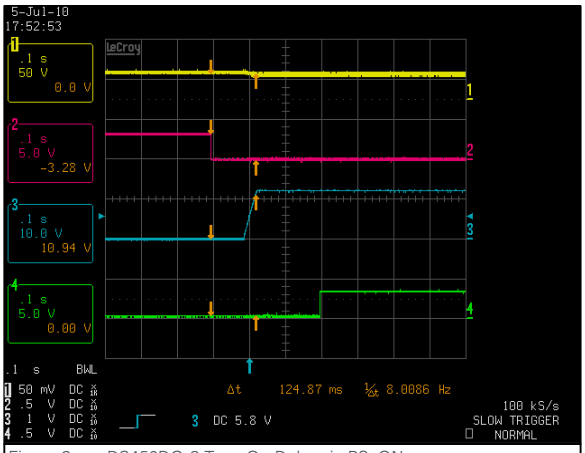


Figure 2: DS450DC-3 Turn-On Delay via PS_ON
Vin = 36Vdc Load: I_O = 37A I_{SB} = 3A (3.3V)
Ch 1: DC Mains Ch 2: PS_ON Ch 3: V_O Ch 4: POK

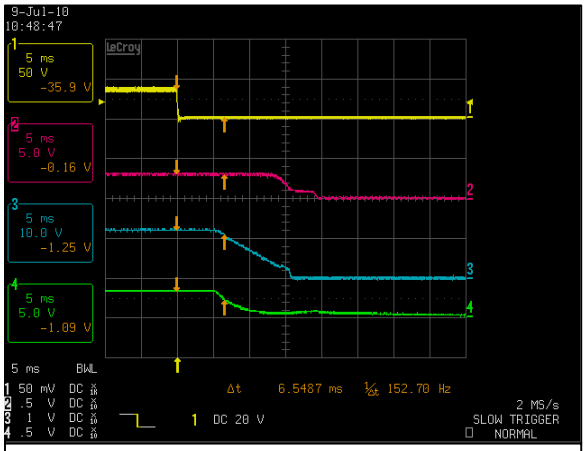


Figure 3: DS450DC-3 Hold-up Time
Vin = 36Vdc Load: Io = 37A I_{SB} = 3A (3.3V)
Ch 1: DC Mains Ch 2: V_{SB} Ch 3: V_O Ch 4: POK

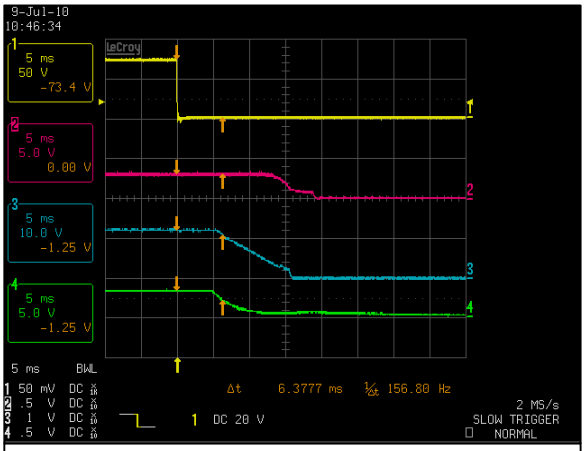


Figure 4: DS450DC-3 Hold-up Time
Vin = 75Vdc Load: Io = 37A I_{SB} = 3A (3.3V)
Ch 1: DC Mains Ch 2: V_{SB} Ch 3: V_O Ch 4: POK

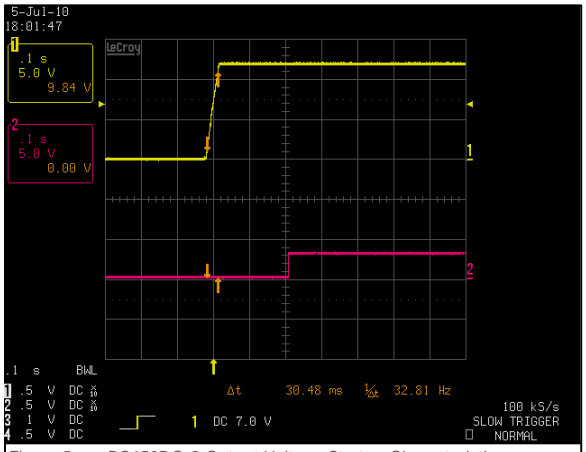


Figure 5: DS450DC-3 Output Voltage Startup Characteristic
Vin = 36Vdc Load: Io = 37A I_{SB} = 3A (3.3V)
Ch 1: V_O Ch 2: POK

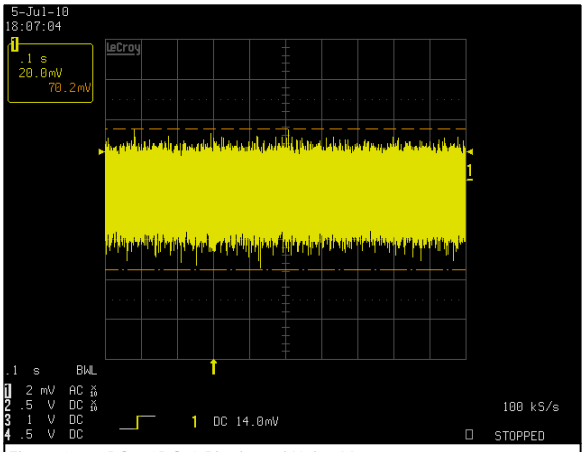


Figure 6: DS450DC-3 Ripple and Noise Measurement
Vin = 36Vdc Load: Io = 37A I_{SB} = 3A (3.3V)
Ch 1: V_O

ELECTRICAL SPECIFICATIONS

DS450DC-3 Performance Curves

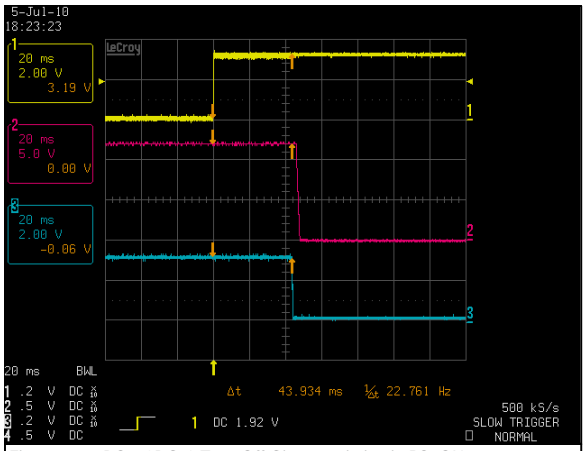


Figure 7: DS450DC-3 Turn Off Characteristic via PS_ON
Load: I_O = 37A I_{SB} = 3A (3.3V)
Ch 1: PS_ON Ch 2: V_O Ch 3: POK

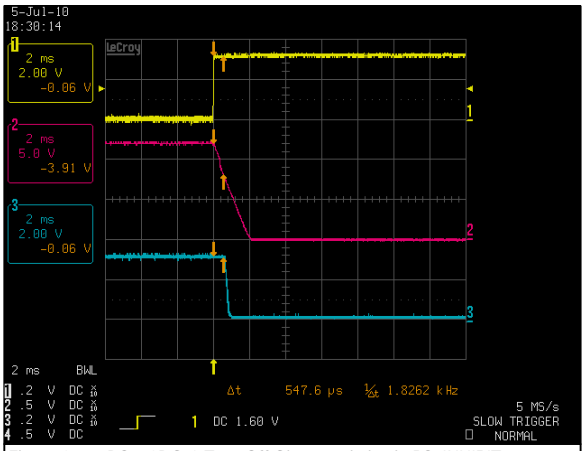


Figure 8: DS450DC-3 Turn Off Characteristic via PS_INHIBIT
Load: I_O = 37A I_{SB} = 3A (3.3V)
Ch 1: PS_INHIBIT Ch 2: V_O Ch 3: POK

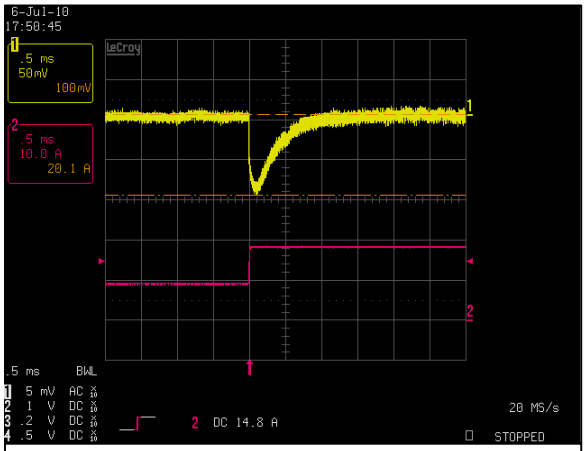


Figure 9: DS450DC-3 Transient Response - V_O Deviation
25% to 50% load change 1A/uS slew rate Vin = 48Vdc
Ch 1: V_O Ch 2: I_O

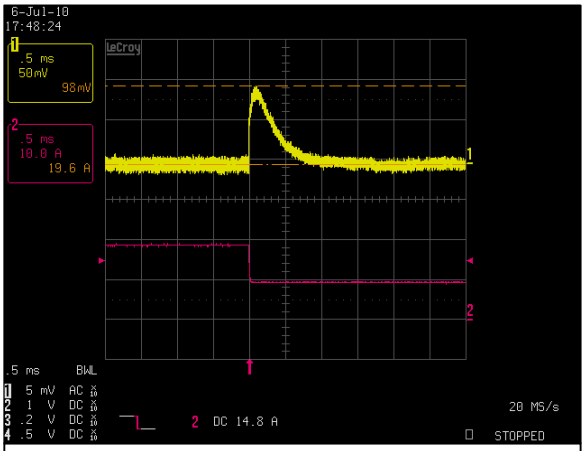


Figure 10: DS450DC-3 Transient Response - V_O Deviation
50% to 25% load change 1A/uS slew rate Vin = 48Vdc
Ch 1: V_O Ch 2: I_O

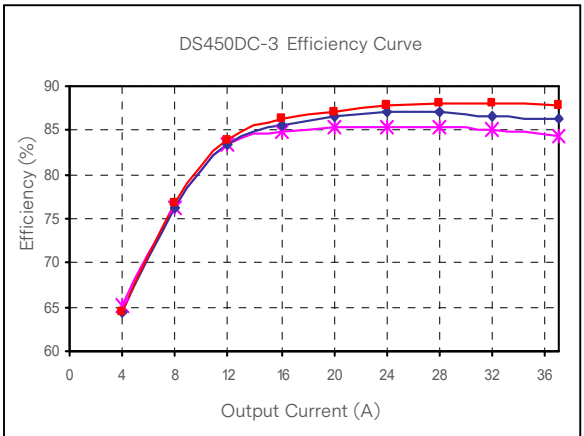


Figure 11: DS450DC-3 Efficiency Curve @ 25°C
36Vdc 48Vdc 75Vdc
Loading: 4A increment to 37A, I_{SB} = 3A (3.3V)

ELECTRICAL SPECIFICATIONS

Protection Function Specifications

Input Fuse

DS450DC-3 series power supply is equipped with an internal primary fuse shall be provided to protect against catastrophic failures. The FKS-80 is an ATO style blade fuse rated at 80V/25A for fault protection in series input lines.

Over Voltage / Under Voltage Protection (OVP / UVP)

The power supply latches off during output overvoltage with the DC line recycled to reset the latch.

OVP

Parameter	Min	Nom	Max	Unit
V_O Output Overvoltage	13.5	/	15.0	V
$3.3V_{SB}$ Output Overvoltage	3.76	/	4.30	V

UVP

Parameter	Min	Nom	Max	Unit
V_O Output Under-voltage	10.5	/	11.0	V
3.3 V_{SB} Output Under-voltage	2.77	/	3.0	V

Over Current Protection (OCP)

DS450DC-3 series includes internal current limit circuitry to prevent damage in the event of overload or short circuit. If the overload is >105% of rated load, the power supply will latch off immediately. Overcurrent protection shall be activated within 20mS on all outputs. Fault latches can be cleared and restarted by recycling DC power or toggling PS_ON. When the +$3.3V_{SB}$ is up to 3.2A to 6A, the output may go into “Auto recovery mode.”

OCP

Parameter	Input Voltage	Min	Nom	Max	Unit
V_O Output Overcurrent	36Vdc	39.5	/	44.4	A
	75Vdc	38.5	/	48.4	A
$3.3V_{SB}$ Output Overvoltage	36Vdc	3.2	/	7	A
	75Vdc	3.2	/	7	A

ELECTRICAL SPECIFICATIONS

Short Circuit Protection (SCP)

A short circuit, which is defined as an impedance of 0.1 ohms or less, applied to any output during start-up or while running will not cause any damage to the power supply such as connectors, components, PCB traces, etc.

When the +3.3V_{SB} is shorted the output may go into “hiccup mode.” When the +3.3V_{SB} attempts to restart the maximum peak current from the output must be less than 10.0A Peak. The maximum average current, taking into account the “hiccup” duty cycle, must be less than 4.9A.

NOTE: Short circuit current from the output caps cannot be controlled.

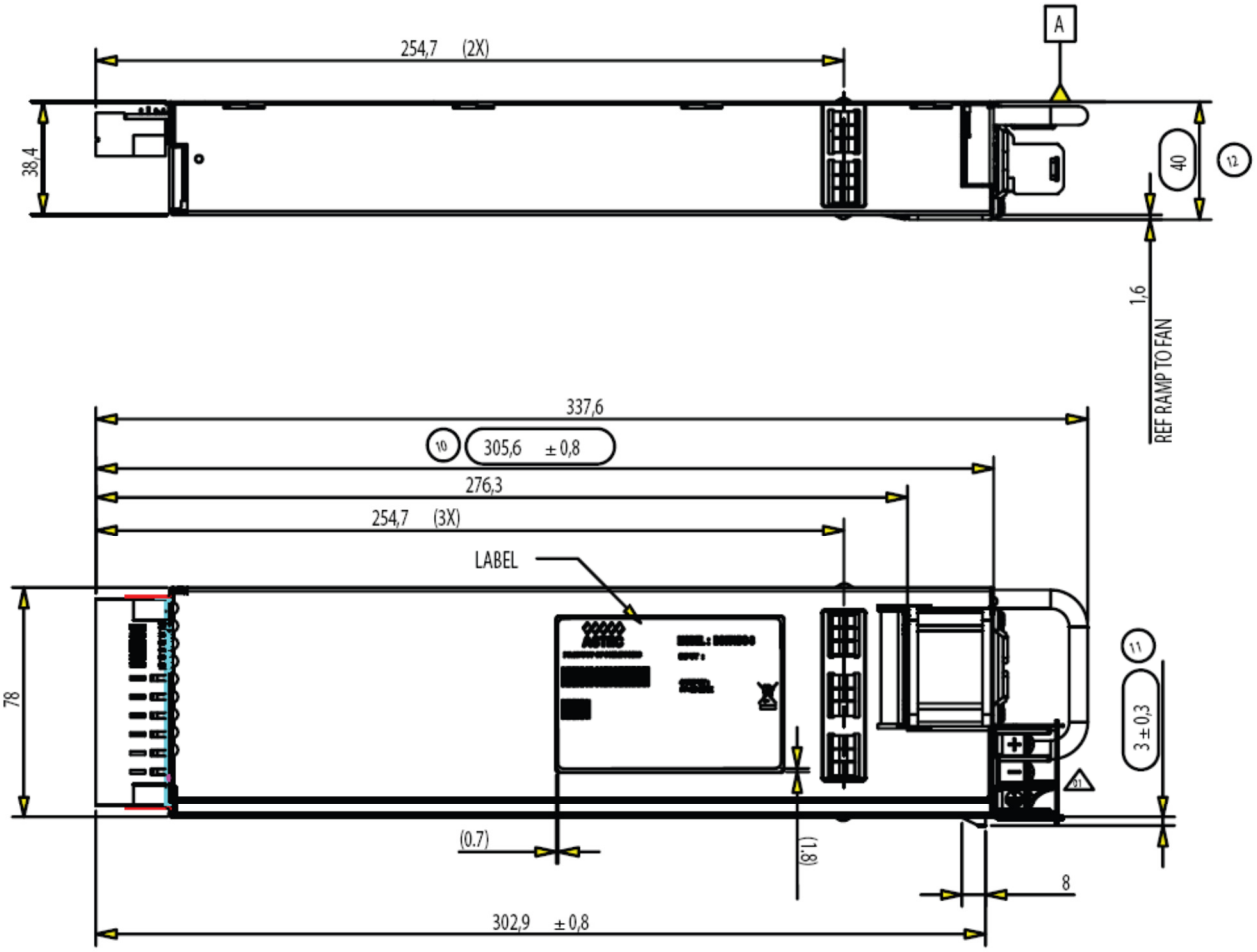
Over Temperature Protection (OTP)

The power supply will incorporate thermal protection to prevent damage or degradation due to overheating.

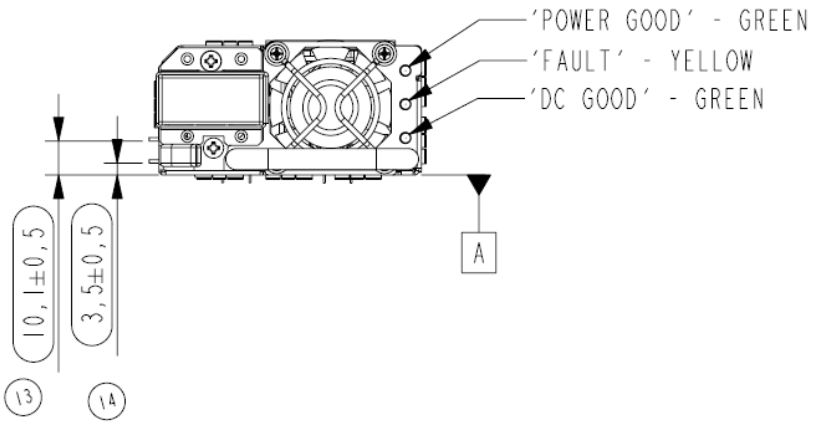
The power supply will be internally protected against over temperature conditions. When the OT circuit is activated, the power supply will shut off. OTP is auto-recovery. This unit shall incorporate both fan speed control, and fan fail.

MECHANICAL SPECIFICATIONS

Mechanical Outlines (DS450DC-3)

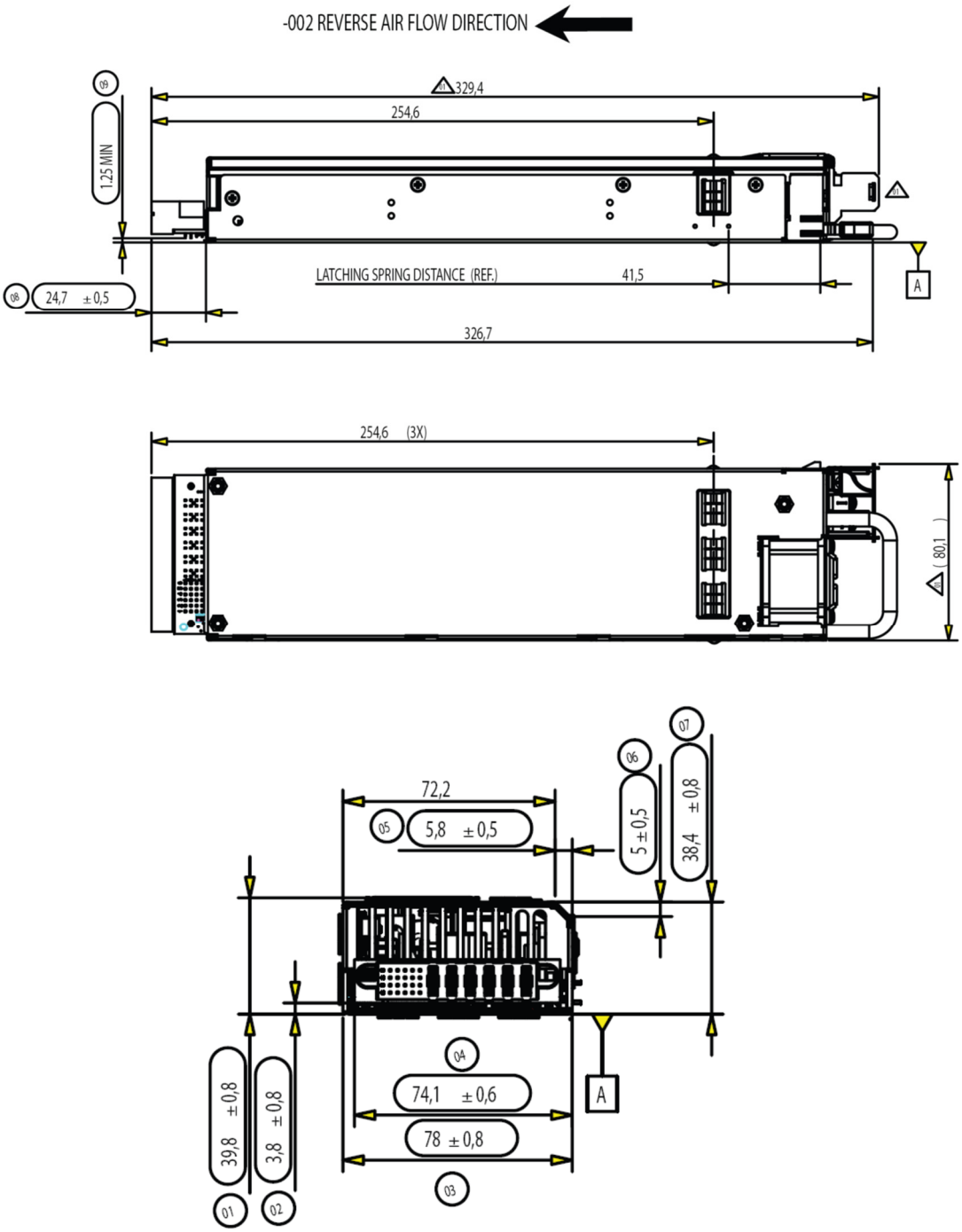


STANDARD AIR FLOW DIRECTION



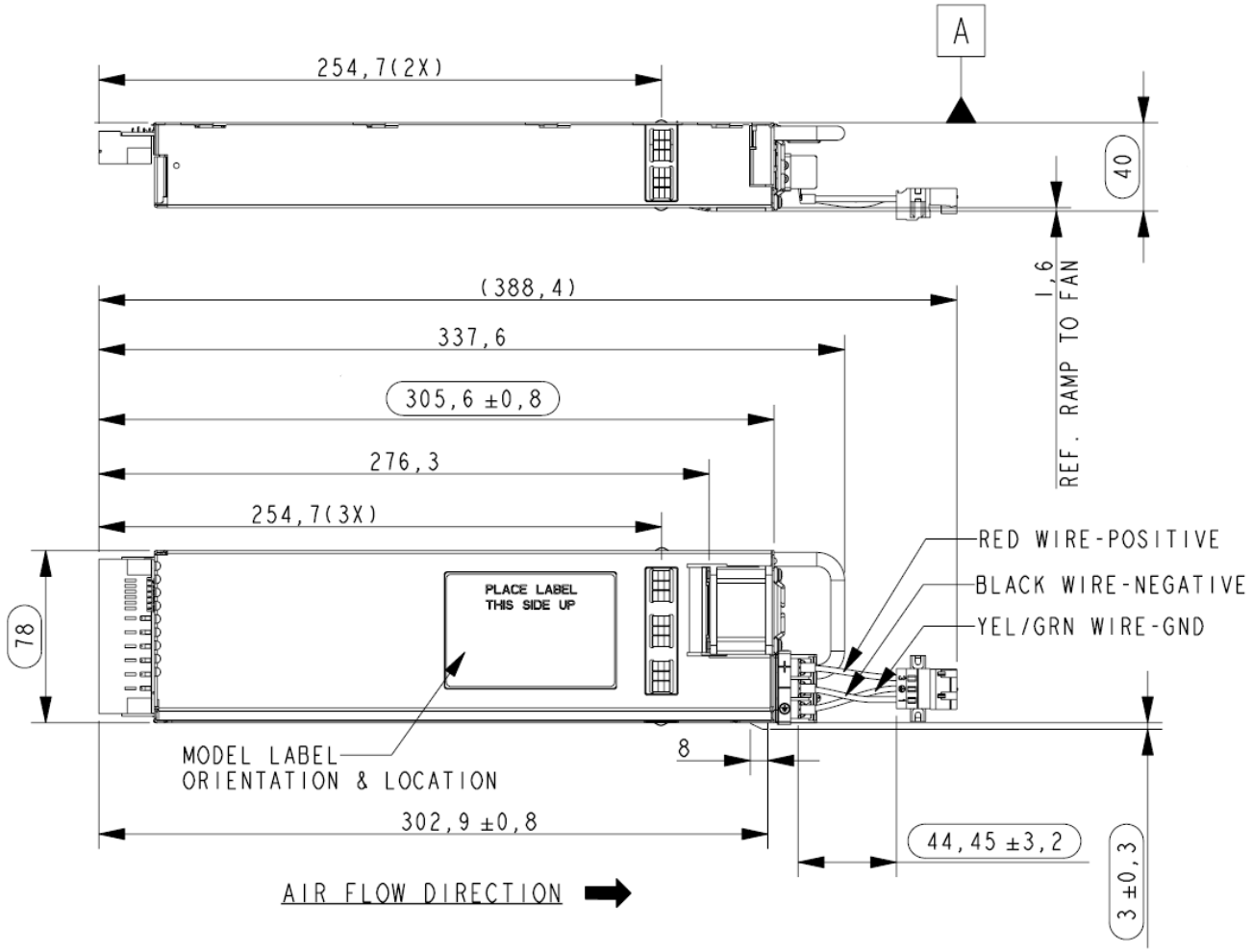
MECHANICAL SPECIFICATIONS

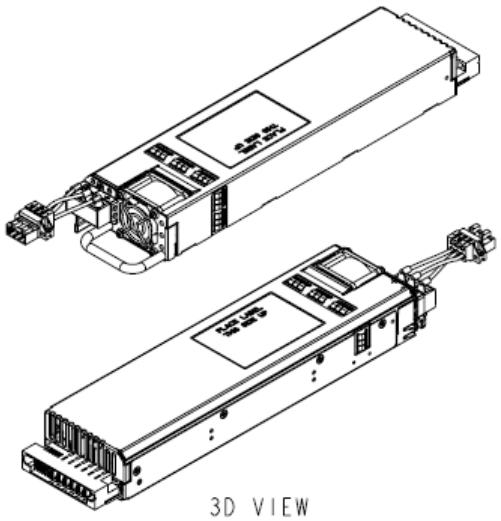
Mechanical Outlines (DS450DC-3-002)



MECHANICAL SPECIFICATIONS

Mechanical Outlines (DS450DC-3-401)





MECHANICAL SPECIFICATIONS

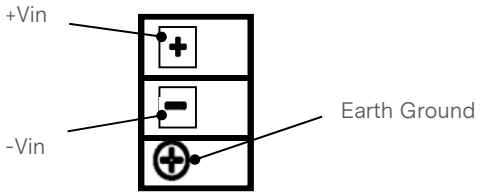
Connector Definitions

DC Input Connector (IEC320 C-16)

Pin 1 – +Vin

Pin 2 – -Vin

Pin 3 – Earth Ground



Output Connector - Power Blades

PB1 – Main Output Return

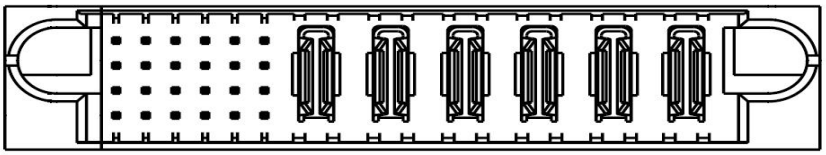
PB2 – Main Output Return

PB3 – Main Output Return

PB4 – Main Output (V_O)

PB5 – Main Output (V_O)

PB5 – Main Output (V_O)



View from power supply output connector end

D1	D2	D3	D4	D5	D6	PB1	PB2	PB3	PB4	PB5	PB6
C1	C2	C3	C4	C5	C6						
B1	B2	B3	B4	B5	B6						
A1	A2	A3	A4	A5	A6						

Output Connector - Control Signals

A1 – PS_KILL
A2 – +12V_Current Share
A3 – Return
A4 – Write Protect
A5 – PS A0 (I^2C Address BIT 0 Signal)
A6 – +3.3VSB
B1 – Return
B2 – +12V RTN Sense
B3 – Return
B4 – +3.3VSB
B5 – SDA (I^2C Data Signal)
B6 – -PS_ON/L
C1 – Return
C2 – Tach_1
C3 – Return
C4 – +3.3VSB
C5 – SCL (I^2C Data Signal)
C6 – VIN_GOOD/H
D1 – -Present/L
D2 – +12V_Sense
D3 – Return
D4 – +3.3VSB
D5 – Alert/L (S_INT)
D6 – POK/H (PWROK/H)

MECHANICAL SPECIFICATIONS

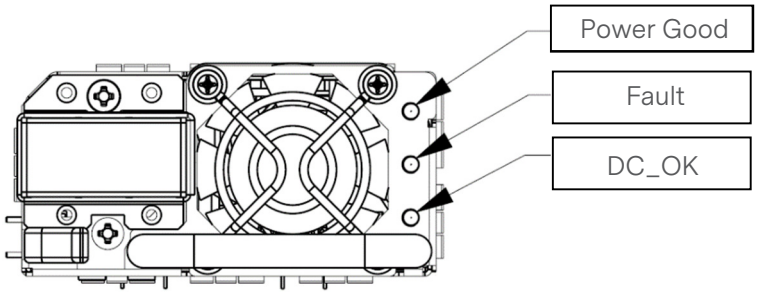
Power / Signal Mating Connectors and Pin Types

Table 5. Mating Connectors for DS450DC-3 Series		
Reference	On Power Supply	Mating Connector or Equivalent
DC Input Connector (DS450DC-3)	DINKLE DT-4C-B02W-03 Center Spacing: 9.5 mm Screw Size: Steel, M3.5, Nickel plated Distance Between Barriers: (8.2 mm)	Wire Range: #12-22 AWG CU
DC Input Connector (DS450DC-3-401)	WAGO 721-603/019-042 No. of Pole: 3 Pin Spacing: 5.0 mm / 0.197 in	WAGO 721-103/026-000 or 721-103/037-000
Output Connector	FCI Power Blade 51721-10002406AA or Molex Power Connector 87667-7002	FCI Power Blade 51741-10002406CC Strait Pins
		FCI Power Blade 51761-10002406AA Right Angle Pins

MECHANICAL SPECIFICATIONS

LED Indicator Definitions

Three LED at the power supply front provides status signal. The status LED conditions is shown on the below table.



Conditions	LED Status
V_{SB} = ON, V_O = OFF, DC Input = ON	DC_OK Solid Green
V_{SB} = ON, V_O = ON	Power Good Solid Green, DC_OK Solid Green
V_O = OCP / UVP / OVP	Solid Amber
FAN_FAULT / OTP / V_{SB} = OCP/UVP	Solid Amber

MECHANICAL SPECIFICATIONS

Weight

The DS450DC-3 series power supply weight is 2.6lbs maximum.

ENVIRONMENTAL SPECIFICATIONS

EMC Immunity

DS450DC-3 series power supply is designed to meet the following EMC immunity specifications.

Table 6. Environmental Specifications

Document	Description
FCC Docket No. 20780 Part 15 Subpart J Class A / EN55032, Level A	Conducted and Radiated EMI Limits
IEC/EN61000-4-2, Edition 1.2, 2001-04	Electromagnetic Compatibility (EMC) - Testing and measurement techniques - Electrostatic discharge immunity test: +/-15KV air, +/-8KV contact discharge. Performance - Criteria B
IEC/EN61000-4-3, 2002, Amendment 1, 2002-08	Electromagnetic Compatibility (EMC) - Testing and measurement techniques - Radiated, radio-frequency, electromagnetic field immunity test: 80 - 1000 MHz, 10V/m, AM 80% (1KHz), 900MHz, 10V/M, PM 100% (200Hz). Performance - Criteria A.
IEC/EN61000-4-4, 1995, Amendment 2, 2001-07	Electromagnetic Compatibility (EMC) - Testing and measurement techniques - Electrical fast transient/burst immunity test: 2KV for AC power port. Performance - Criteria B 1KV for DC ports, I/O and signal ports. Performance - Criteria B
IEC/EN61000-4-5, Edition 1.1, 2001-04	Electromagnetic Compatibility (EMC) - Testing and measurement techniques - Surge test: 2KV common mode and 1KV differential mode for AC ports and 0.5KV differential mode for DC power, I/O and signal ports. Performance - Criteria B
EN55024:1998	Information Technology Equipment - Immunity Characteristics, Limits and Method of Measurements

ENVIRONMENTAL SPECIFICATIONS

Safety Certifications

The DS450DC-3 series power supply is intended for inclusion in other equipment and the installer must ensure that it is in compliance with all the requirements of the end application. This product is only for inclusion by professional installers within other equipment and must not be operated as a stand alone product.

Table 7. Safety Certifications for DS450DC-3 Series Power Supply

Document	File #	Description
UL62368		US and Canada Requirements
CSA 22.2 No. 62368		Information Technology Equipment - Safety - Part 1: General Requirements (Bi-National standard, with UL62368-1)
EN62368		European Requirements
EN62368 Deviations		International Requirements
CB Certificate and Report	46478	(All CENELEC Countries)
CE Mark	P08208864	LVD
CHINA CCC Approval	2008010907302876	China Requirements
UKCA Mark		UK Requirements

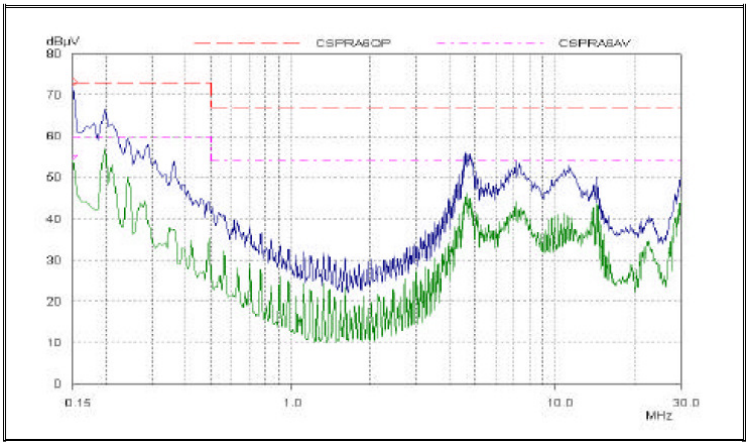
ENVIRONMENTAL SPECIFICATIONS

EMI Emissions

The DS450DC-3 series has been designed to comply with the Class A limits of EMI requirements of EN55032 (FCC Part 15) and CISPR 22 (EN55032) for emissions and relevant sections of EN61000 (IEC61000) for immunity. The unit is enclosed inside a metal box, tested at 450W using resistive load with cooling fan.

Conducted Emissions

The applicable standard for conducted emissions is EN55032 (FCC Part 15). Conducted noise can appear as both differential mode and common mode noise currents. Differential mode noise is measured between the two input lines, with the major components occurring at the supply fundamental switching frequency and its harmonics. Common mode noise, a contributor to both radiated emissions and input conducted emissions, is measured between the input lines and system ground and can be broadband in nature.



The DS450DC-3 power supplies have internal EMI filters ensure the convertors' conducted EMI levels comply with EN55032 (FCC Part 15) Class A and EN55032 (CISPR 22) Class A limits. The EMI measurements are performed with resistive loads at maximum rated loading.

Sample of EN55032 Conducted EMI Measurement at 48Vdc input

Note: Red Line refers to Artesyn Quasi Peak margin, which is 6dB below the CISPR international limit. Pink Line refers to the Artseyn Average margin, which is 6dB below the CISPR international limit.

Table 8. Conducted EMI Emission Specifications of The DS450DC-3 Series Power Supply

Parameter	Model	Symbol	Min	Typ	Max	Unit
FCC Part 15, class A	All	Margin	-	-	6	dB
CISPR 22 (EN55022) class A	All	Margin	-	-	6	dB

ENVIRONMENTAL SPECIFICATIONS

Radiated Emissions

Unlike conducted EMI, radiated EMI performance in a system environment may differ drastically from that in a stand-alone power supply. The shielding effect provided by the system enclosure may bring the EMI level from Class A to Class B. It is thus recommended that radiated EMI be evaluated in a system environment. The applicable standard is EN55032 Class A (FCC Part 15). Testing AC-DC convertors as a stand-alone component to the exact requirements of EN55032 can be difficult, because the standard calls for 1m leads to be attached to the input and outputs and aligned such as to maximize the disturbance. In such a set-up, it is possible to form a perfect dipole antenna that very few AC-DC convertors could pass. However, the standard also states that an attempt should be made to maximize the disturbance consistent with the typical application by varying the configuration of the test sample.

ENVIRONMENTAL SPECIFICATIONS

Operating Temperature

The DS450DC-3 series power supplies will start and operate within stated specifications at an ambient temperature from -10°C to 50°C under all load conditions with internal fan.

Forced Air Cooling

The fan(s) will be included as part of the power supply assembly and provide forced air-cooling of desired CFM to maintain or control temperature of devices and ambient temperature in the power supply to appropriate levels. The standard direction of airflow shall be from the DC connector end to the DC end of the power supply. It can be reverse the airflow direction.

ENVIRONMENTAL SPECIFICATIONS

Storage and Shipping Temperature / Humidity

The DS450DC-3 series power supply can be stored or shipped at temperatures between -40°C to +85°C and relative humidity up to 95% non-condensing.

Altitude

The DS450DC-3 series power supply will operate within specifications at altitudes up to 10,000 feet above sea level. The power supply will not be damaged when stored at altitudes of up to 35,000 feet above sea level.

Humidity

The DS450DC-3 series power supply will operate within specifications when subjected to a relative humidity from 20% to 90% non-condensing. The DS450DC-3 series can be stored in a relative humidity up to 95% non-condensing.

Vibration

The DS450DC-3 series power supply will pass the following vibration specifications:

Non-Operating Random Vibration

Acceleration	2.5		gRMS
Frequency Range	10 - 2000		Hz
Duration	20		Mins
Direction	3 mutually perpendicular axis		
PSD Profile	**FREQ (Hz)**	**SLOPE (db/oct)**	**PSD (g^2/Hz)**
	10 - 200	/	0.01
	200 - 2000	/	0.003

Operating Random Vibration

Acceleration	1.0		gRMS
Frequency Range	10 - 2000		Hz
Duration	20		Mins
Direction	3 mutually perpendicular axis		
PSD Profile	**FREQ (Hz)**	**SLOPE (db/oct)**	**PSD (g^2/Hz)**
	10 - 2000	/	0.02

ENVIRONMENTAL SPECIFICATIONS

Shock

The DS450DC-3 series power supply will pass the following vibration specifications:

Non-Operating Half-Sine Shock

Acceleration	30	G
Duration	18	mSec
Pulse	Half-Sine	
Number of Shock	3 shocks in each of 6 faces	

Operating Half-Sine Shock

Acceleration	4	G
Duration	22	mSec
Pulse	Half-Sine	
Number of Shock	3 shocks in each of 6 faces	

POWER AND CONTROL SIGNAL DESCRIPTIONS

DC Input Connector

This connector supplies the DC to the DS450DC-3 power supply.

Pin1 – +Vin
Pin2 – -Vin
Pin3 – Earth Ground

Output Connector – Power Blades

These pins provide the main output for the DS450DC-3 series power supply. The main output (V_O) and the main output return pins are the positive and negative rails, respectively, of the V_O main output of the DS450DC-3 series power supply. The main output (V_O) is electrically isolated from the power supply chassis.

PB1 – 12V Main Output Return
PB2 – 12V Main Output Return
PB3 – 12V Main Output Return
PB4 – 12V Main Output (V_O)
PB5 – 12V Main Output (V_O)
PB6 – 12V Main Output (V_O)

Output Connector – Control Signals

The DS450DC-3 series power supply contains a 24 pins control signal header analogy control interface, standby power and I^2C interface signal connections.

PS_KILL - (Pin A1)

The PS_KILL input is separate from the PS_ON input and is connected directly and only to the system cover interlocks. The DC 12V output will be disabled only when the input is driven higher than 2.4V, or open circuited. PS_KILL will cause the PSU to latch off the main 12V output rail. Recycling PS_ON or recycling the DC supply can clear this latch. There shall be a pull up resistor (10K-Ref) located within the PSU to +3.3VSB or internal housekeeping supply. When hot plugging or hot unplugging the power supply, the PS_KILL signal shall not cause the power supply to FAULT or LATCH-OFF.

+12V_Current Share - (Pin A2)

The DS450DC-3 supports active current sharing through a single wire force current share shall be employed on the +12V output. When one or more power supplies are connected and operating in parallel and each is delivering 50% or more of its rated output to the load, the power supplies shall current share within 10% accuracy, between 50% - 100% load. When supplying light loads between 10% and 20% of its rated load, the power supplies shall share within 20% accuracy. If any power supply is hot swapped, no glitch shall occur that violates the regulation limits of the power supply defined in this specification. Recommend the use of the ADM1041 IC.

Compute current share voltage using formula below:

IShare bus voltage = (output current * 8.0V) / 12V full load current.

+3.3VSB, StandBy Output Return - (Pins A3, A6, B1, B3, B4, C1, C3, C4, D3, D4)

The DS450DC-3 provides a regulated 3.3 volt 3 amp (or 5.0 volt 2 amp) auxiliary output voltage to power critical circuitry that must remain active regardless of the on/off status of the power supply's main output. The Standby Output (VSB) voltage is available whenever a valid DC input voltage is applied to the unit. The StandBy Output is independently short circuit protected and is referenced to the StandBy Output Return pins (A3, B1, B3, C1, C3, D3).

POWER AND CONTROL SIGNAL DESCRIPTIONS

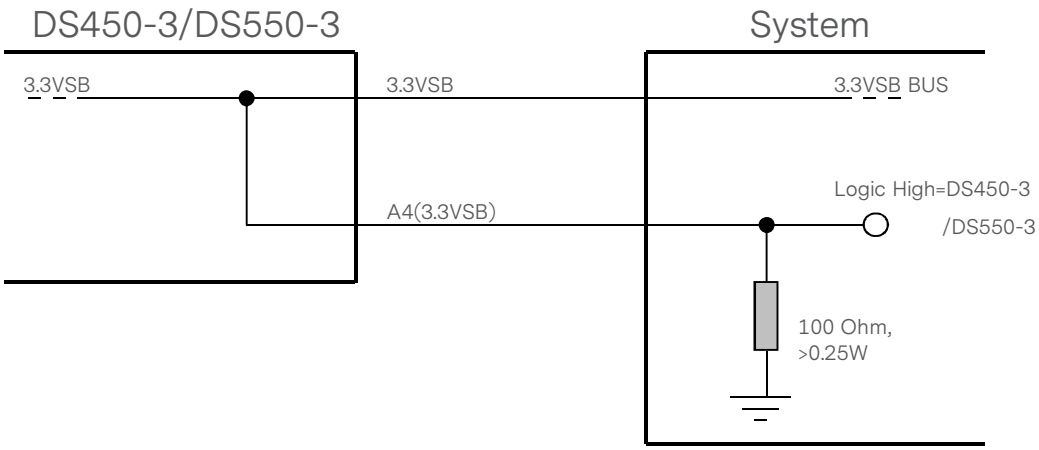
Write Protect - (Pin A4)

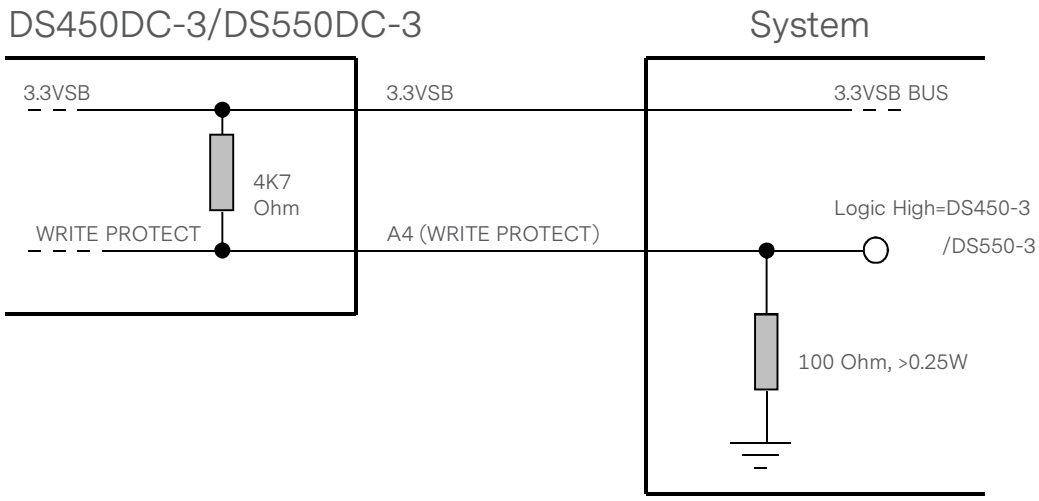
The write protect pin allows or denies write access to the whole of the EEPROM memory array. Attempts to write to the EEPROM when the write protection is active will be acknowledged by the EEPROM but ignored.

To protect the EEPROM memory this pin is may be left open or pulled to +3.3VSB by the system and shall have an internal pull-up or 4K7ohms or higher to the shared + 3.3VSB in the power supply.

To allow write to the EEPROM memory the signal has to be pulled low. As physically compatible power supplies exist that connect the same connector pin (A4) to 3.3VSB inside the power supply it is recommended that a 100 ohm 0.25W minimum resistor is used to pull the signal to 0V to allow for these parts to be fitted accidentally.

To accommodate both DS450-3/DS550-3 and DS450DC-3/DS550DC-3, system can be configured as below. In such case, A4 pin can be used to detect PSU type where “Logic High” indicate DS450-3/DS550-3 and “Logic Low” indicate DS450DC-3/DS550DC-3.





POWER AND CONTROL SIGNAL DESCRIPTIONS

PS A0 - (Pin A5)

Please refer to “Communication Bus Descriptions” section.

+12V RTN Sense, +12V_Sense - (Pins B2, D2)

The main output of the DS450DC-3 is equipped with a remote sensing capability that will compensate for a power path drop around the entire loop of 0.2 volt. This feature is implemented by connecting the +12V_Sense (pin D2) and the +12V RTN Sense (pin B2) to the positive and negative rails of the main output, respectively, at a location that is near to the load. The DS450DC-3 will operate appropriately without the sense lines connected; however it is recommended that the sense lines be connected directly to the main output terminals if remote sensing is not required. This remote sense circuit will not raise the power supply’s output voltage to the OVP trip level. Main output remote sense has no effect on the standby output (V_{SB}).

SDA, SCL and S_INT - (Pins B5, C5, D5)

Please refer to “Communication Bus Descriptions” section.

PS_ON/L - (Pin B6)

This signal input pin controls the normal turning ON and Off of the main output of the DS450DC-3 power supply. The power supply 12VDC output will be enabled when this signal is pulled low, below 0.8V. In the low state the input will not source more than 1mA of current. The 12VDC output will be disabled when the input is driven higher than 2.4V, or open circuited.

PS_ON is an active LOW signal controlled by the system (via I^2C bus) and pulled up internal to PSU +3.3VSB rail or internal house keeping supply.

HIGH = Output V1 OFF (disabled) LOW = Output V1 ON (enabled)

Tach_1 - (Pin C2)

This signal is generated from the fan. The signal should generate 2 pulses per revolution. The logic in the system will be operating at 3.3V. The TACH output is open collector and will have an internal pull-up resistor to +3.3VSB or internal housekeeping supply. There must also be a provision for pull up resistor to be taken from either 3.3V / 5V at system side.

VIN_GOOD/H - (Pin C6)

Active high signal asserted when the input voltage rises above the min input voltage specified. This signal is internally pulled up through 4.7K ohms to the 3.3V housekeeping voltage.

The hold up requirement shall be met at -36 VDC input. High = OK, Low = Supply out of range. The output will be an open collector/drain. It will be capable of driving the output below 0.4V with a load of 4mA.

-Present/L - (Pin D1)

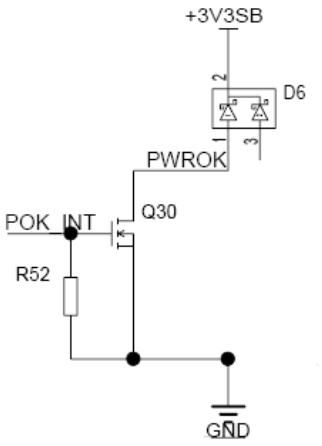
This signal is used to detect the presence of a PSU by the system. The signal is pulled up within the system and connected direct to the PSU Logic GND.

HIGH = PSU not present LOW = PSU present

POWER AND CONTROL SIGNAL DESCRIPTIONS

POK/H (PWROK/H) - (Pin D6)

The POK is an output signal driven high, by the power supply to indicate that all outputs are valid. If any of the power supply outputs fails below its regulation limits, this output will be driven low. The output signal is an open drain output internally pulled up in the power supply to internal standby supply (anode side of standby output or'ing circuit) via a diode. It is capable of driving the output below 0.4V with a load of 4mA.



COMMUNICATION BUS DESCRIPTIONS

I²C Bus Signals

The DS450DC-3 power supply contains monitor functions implemented via the I²C bus. The DS450DC-3 I²C functionality (EEPROM for FRU data) can be accessed via the output connector control signals. The communication bus is powered either by the internal 3.3V supply or from an external power source connected to the standby output (ie: accessing an unpowered power supply as long as the standby output of another power supply connected in parallel is on).

If units are connected in parallel or in redundant mode, the standby outputs must be connected together in the system. Otherwise, the I²C bus will not work properly when a unit is inserted into the system without the AC source connected.

Note: PMBus™ functionality can be accessed only when the PSU is powered up. Guaranteed communication I²C speed is 100KHz.

SDA, SCL (I²C Data and Clock Signals) - (Pins B5, C5)

I²C serial data and clock bus - these pins are internally pulled up to internal 3.3V supply with a 10Kohm resistor. and located within the PSU, and de-coupled with 100pF and 100ohm maximum series resistor to the system.

S_INT (Alarm) - (Pin D5)

S_INT is used to send a signal to the system that a fault in the power supply occurred. This signal is normally logic level HIGH. It will go to a LOW logic level when a fault bit has been set in the power supply's status register. To reset the S_INT signal back to normal (logic HIGH level) - (1) recycle input DC power, (2) toggle PSON signal and (3) issuance of a CLEAR_FAULTS PMBus™ command.

PS A0 (I²C Address BIT 0) - (Pin A5)

The input pins is the address lines A0 to indicate the slot position the power supply occupies in the power bay and define the power supply addresses for FRU data communication. This allows the system to assign different addresses for each power supply. During I²C communication between system and power supplies, the system will be the master and power supplies will be slave.

They are internally pulled up to internal 3.3V supply with a 4.7K resistor.

I²C Bus Communication Interval

The interval between two consecutive I²C communications to the power supply must be at least 50ms to ensure proper monitoring functionality.

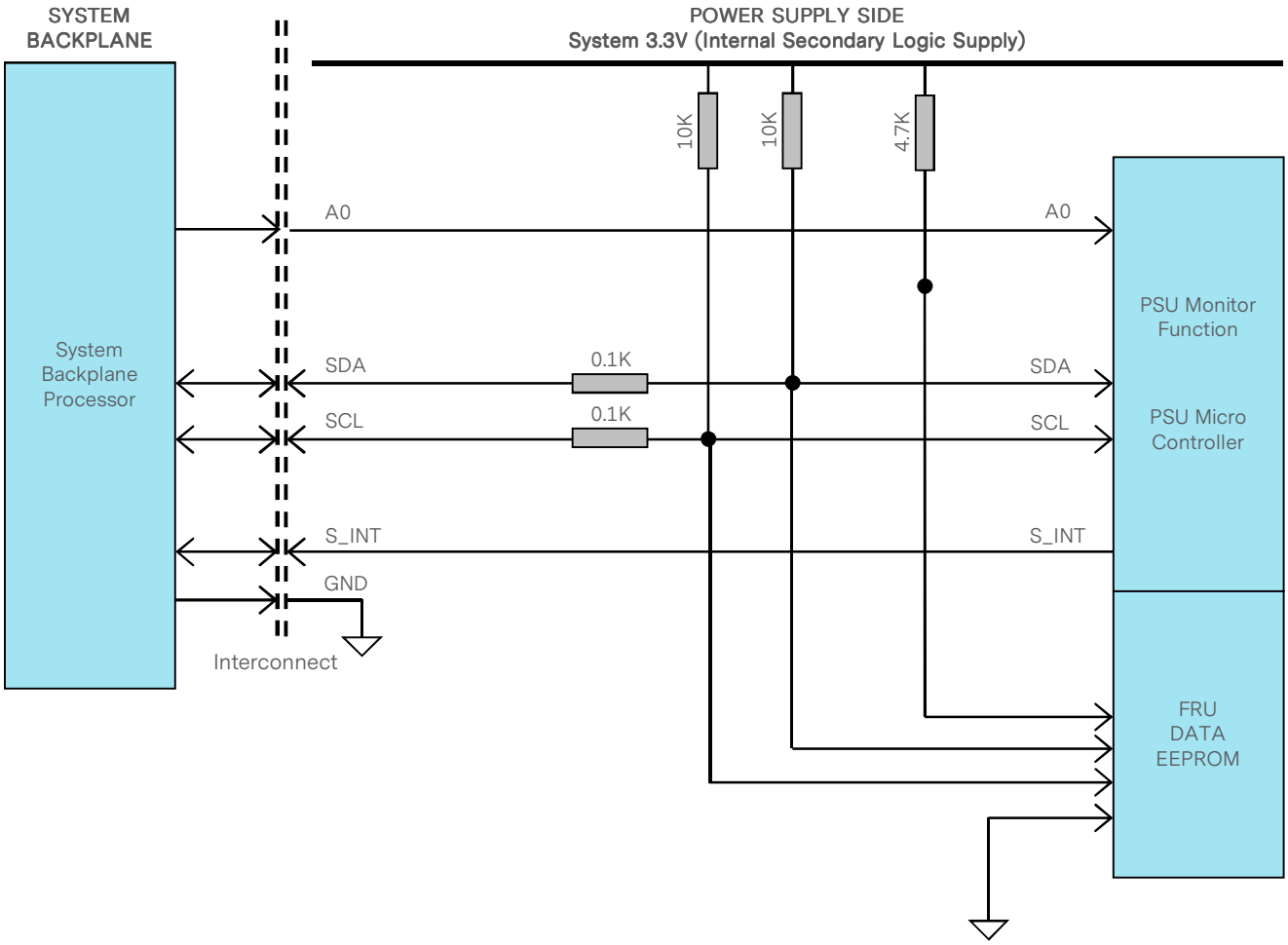
I²C Bus Signal Integrity

The noise on the I²C bus (SDA, SCL lines) due to the power supply will be less than 500mV peak-to-peak. This noise measurement should be made with an oscilloscope bandwidth limited to 100MHz. Measurements should be make at the power supply output connector with 3.2Kohm resistors pulled up to standby output and 20pf ceramic capacitors to standby output return.

The noise on the address lines A0 will be less than 100mV peak-to-peak. This noise measurement should be made at the power supply output connector.

COMMUNICATION BUS DESCRIPTIONS

I²C Bus Internal Implementation, Pull-ups and Bus Capacitances



I²C Bus - Recommended external pull-ups

Electrical and interface specifications of I²C signals (referenced to standby output return pin, unless otherwise indicated):

Parameter	Condition	Symbol	Min	Type	Max	Unit
SDA, SCL Internal Pull-up Resistor		R_{int}	-	10	-	Kohm
SDA, SCL internal bus capacitance		C_{int}	-	100	-	pF
Recommended External Pull-up Resistor	1 PSU	R_{ext}	-	-	-	Kohm
	2 PSU	R_{ext}	-	-	-	Kohm

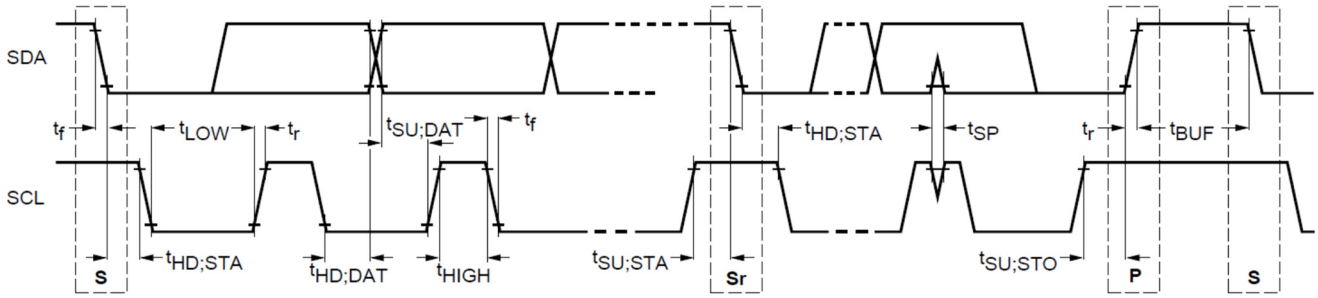
COMMUNICATION BUS DESCRIPTIONS

Logic Levels

DS450DC-3 series power supply I²C communication bus will respond to logic levels as per below:

Logic High: 3.3V nominal (Spec is 2.1V to 5.5V)
Logic Low: 500mV nominal (Spec is 800mV max)

Timings



Parameter	Symbol	Standard-Mode Specs		Actual Measured		Unit
		Min	Max			
SCL clock frequency	f_{SCL}	0	100	99.8		KHz
Hold time (repeated) START condition	$t_{HD;STA}$	4.0	-	13.8		uS
LOW period of SCL clock	t_{LOW}	4.7	-	25.8		uS
HIGH period of SCL clock	t_{HIGH}	4.0	50	8.1		uS
Setup time for repeated START condition	$t_{SU;STA}$	4.7	-	14.3		uS
Data hold time	$t_{HD;DAT}$	0	3.45	1.59		uS
Data setup time	$t_{SU;DAT}$	250	-	9763		nS
Rise time	t_r	-	1000	SCL = 845	SDA = 983	nS
Fall time	t_f	-	300	SCL = 95	SDA = 97	nS
Setup time for STOP condition	$t_{SU;STO}$	4.0	-	10.1		uS
Bus free time between a STOP and START condition	t_{BUF}	4.7	-	58.5		uS

*** Note - Win-I²CNT adapter (Parallel port-to-I²C) and Win-I²CNT GUI software was used.

COMMUNICATION BUS DESCRIPTIONS

Device Addressing

The DS450DC-3 series will respond to supported commands on the I^2C bus that are addressed according to A0 pin of output connector.

Address pins are held HIGH by default via pulled up to internal 3.3V supply with a 10K resistor. To set the address as “0”, the corresponding address line should be pulled down to logic ground level. Below tables show the address of the power supply with A0 pin set to either “0” or “1”:

PSU Slot	Slot ID Bits	Read Address	EEPROM(FRU) Read Address
	A0		
1	0	0x7D	0xAD
2	1	0x7F	0xAF

Note - Default address when A0 is left open.

COMMUNICATION BUS DESCRIPTIONS

Power Supply Status Register 0x7Eh

Power supply status monitoring can be done via the status register 0x7Eh or as I/O expander. Detailed explanation of functions is given below:

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
DC PRFAIL	PS STATUS	P_Good	Vin_Good	OV 12V	UV 12V	Fan Fault	OC 12V

- DC_PRFAIL
  - Power Drop Detection
  - the bit is high except when the power supply turns the main outputs, not +3.3VSB, off due to a DC failure the supply is turned off due to PS_ON, PS_KILL, or a fault, then P7 remains high.
- PS_STATUS
  - Power Supply Status
  - A logic low, when the power supply is off, either due to PS_ON,PS_KILL or a fault, the bit is high
- P_Good
  - Main Output (V_O) Status
  - This bit will be set when the power supply outputs have been disabled due to an over voltage event.
- Vin_Good
  - DC Line Voltage Status
  - This bit is an image of the DC_OK signal coming out the power supply to the system. A logic HIGH, if the input voltage is within allowable limits.
- OV +12V
  - Over Voltage Protection
  - This bit will be low set when the power supply outputs have been disabled due to an over voltage event.
- UV +12V
  - Under Voltage Protection
  - This bit will be set low when the power supply outputs have been disabled due to an under voltage event.
- Fan Fault
  - Fan Status
  - Any abnormalities on the fan will clear this bit. Normal fan operation, this is set to high.
- OV +12V
  - Over Current Protection
  - This bit will be set when the power supply outputs have been disabled due to an over current event.

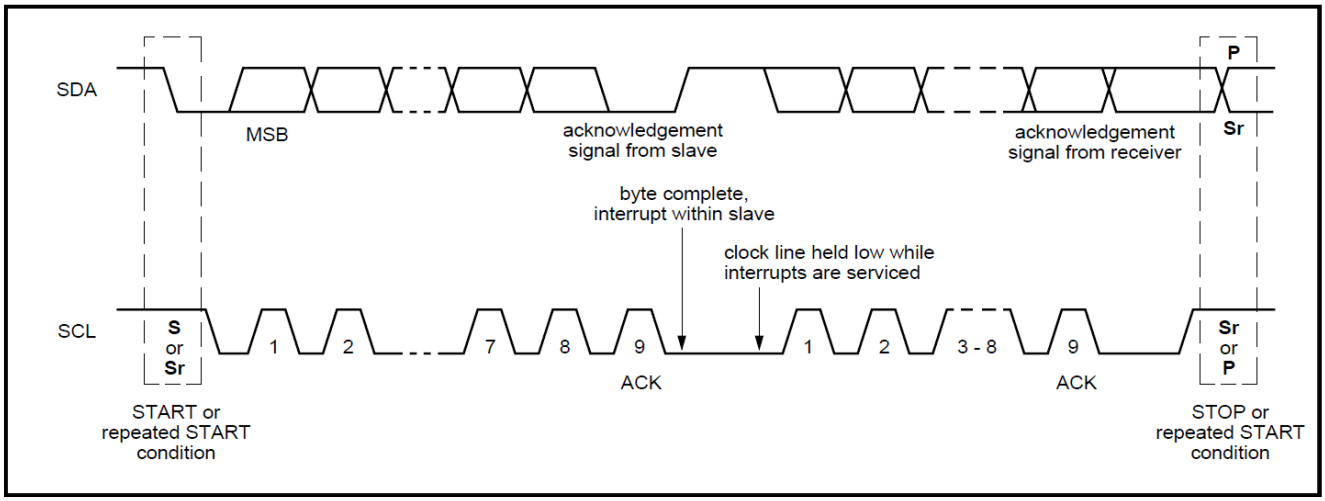
Status Register Code		
Signal Name	**Code (Binary)**	**Code (Hex)**
Normal / 12V ON	10111111	BF
Normal / 12V OFF	11011111	DF
OCP	11011110/11011010	DE / DA
UVP	11001111	CF
NO DC	11001111	CF
DC PRFAIL	01011111/01001111	5F / 4F

COMMUNICATION BUS DESCRIPTIONS

I²C Clock Synchronization

The DS450DC-3 series power supply applies clock stretching. An addressed slave power supply holds the clock line (SCL) low after receiving (or sending) a byte, indicating that it is not yet ready to process more data. The system master that is communicating with the power supply will attempt to raise the clock to transfer the next bit but must verify that the clock line was actually raised. If the power supply is clock stretching, the clock line will still be low (because the connections are open-drain).

The maximum time-out condition for clock stretching for DS450DC-3 series is 100 milliseconds.



COMMUNICATION BUS DESCRIPTIONS

FRU (EEPROM) Data

The FRU (Field Replaceable Unit) data format is compliant with the Intel IPMI v1.0 specification. The DS450DC-3 uses 1 page of EEPROM for FRU purpose. The one page of EEPROM contains up to 256 byte-sized data locations.

Where: OFFSET -The OFFSET denotes the address in decimal format of a particular data byte within DS450DC-3 EEPROM.

VALUE -The VALUE details data written to a particular memory location of the EEPROM.

DEFINITION -The contents DEFINITION refers to the definition of a particular data byte.

DS450DC-3 series FRU (EEPROM) Data:

OFFSET		DEFINITION	SPEC VALUE	
(DEC)	(HEX)	(REMARKS)	(DEC)	(HEX)
		COMMON HEADER, 8 BYTES		
0	00	**FORMAT VERSION NUMBER** (Common Header) 7:4 - Reserved, write as 0000b 3:0 - Format Version Number = 1h for this specification	1	01
1	01	**INTERNAL USE AREA OFFSET**	24	18
2	02	**CHASSIS INFO AREA OFFSET**	1	01
3	03	**BOARD INFO AREA OFFSET**	0	00
4	04	**PRODUCT INFO AREA OFFSET**	5	05
5	05	**MULTI RECORD AREA OFFSET**	15	0F
6	06	**PAD** (reserved) Default value is 0.	0	00
7	07	**ZERO CHECK SUM** (256 - (Sum of bytes 0 to 6))	210	D2
		CHASSIS INFO AREA (32 BYTES) **This area will be filled by the Mfg. Diag. or by the OS if used**		
8	08	**FORMAT VERSION NUMBER** 7:4 - Reserved, write as 0000b 3:0 - Format Version Number = 1h for this specification	1	01
9	09	**CHASSIS INFO AREA LENGTH** in multiple of 8 bytes	0	00
10	0A	**CHASSIS TYPE** (Default value is 0.)	0	00
11	0B	**CHASSIS PART NUMBER** Type/Length 10-byte allocation Type = “ASCII+LATIN1” = (11)b Length = 10 bytes = (001010)b	0	00
12 13 14 15 16 17 18 19 20 21	0C 0D 0E 0F 10 11 12 13 14 15	**CHASSIS PART NUMBER BYTES** (Default value is 0.)	0 0 0 0 0 0 0 0 0 0	00 00 00 00 00 00 00 00 00 00
22	16	**CHASSIS SERIAL NUMBER Type/Length** 15-byte allocation	0	00
23 24 25 26 27 28 29 30 31 32	17 18 19 1A 1B 1C 1D 1E 1F 20	**CHASSIS SERIAL NUMBER BYTES,** default value is 0.	0 0 0 0 0 0 0 0 0 0	00 00 00 00 00 00 00 00 00 00

COMMUNICATION BUS DESCRIPTIONS

DS450DC-3 series FRU (EEPROM) Data:

OFFSET		DEFINITION	SPEC VALUE	
(DEC)	(HEX)	(REMARKS)	(DEC)	(HEX)
33 34 35 36 37	21 22 23 24 25	**CHASSIS SERIAL NUMBER BYTES,** default value is 0.	0 0 0 0 0	00 00 00 00 00
38	26	**End Tag**	0	00
39	27	**ZERO CHECK SUM** (100H-((Sum of byte 08h-26h) and FFH)	255	FF
		PRODUCT INFORMATION AREA, 80 BYTES		
40	28	**FORMAT VERSION NUMBER** (Product Info Area) 7:4 - Reserved, write as 0000b 3:0 - Format Version Number = 1h for this specification	1	01
41	29	**PRODUCT INFO AREA LENGTH** (In multiples of 8 bytes)	10	0A
42	2A	**Language Code (English)**	25	19
43	2B	**MANUFACTURER NAME TYPE/LENGTH** (0C5H) 7-6: (11)b, 8-bit ASCII + Latin 1, 5-0: (000101)b, 5-byte allocation	197	C5
		MANUFACTURER'S NAME		
44	2C	"A" = 41h	65	41
45	2D	"S" = 53h	83	53
46	2E	"T" = 54h	84	54
47	2F	"E" = 45h	69	45
48	30	"C" = 43h	67	43
49	31	**PRODUCT NAME** Type/Length (0CEH) 7-6: (11)b, 8-bit ASCII + Latin 1, 5-0: (001110)b, 14-byte allocation	206	CE
		PRODUCT NAME		
50	32	"D" = 44H	68	44
51	33	"S" = 53H	83	53
52	34	"4" = 34H	52	34
53	35	"5" = 35H	53	35
54	36	"0" = 30H	48	30
55	37	"D" = 44H	68	44
56	38	"S" = 43H	67	43
57	39	"-" = 2DH	45	2D
58	3A	"3" = 33H	51	33
59	3B	" " = 20H	32	20
60	3C	" " = 20H	32	20
61	3D	" " = 20H	32	20
62	3E	" " = 20H	32	20
63	3F	" " = 20H	32	20
64	40	**PRODUCT PART/MODEL NUMBER** Type/Length (0CAH) 7-6: (11)b, 8-bit ASCII + Latin 1, 5-0: (001010)b, 10-byte allocation	202	CA
65 66 67 68 69 70 71 72 73 74	41 42 43 44 45 46 47 48 49 4A	**POWER SUPPLY SPARE KIT NUMBER** Power Supply Spare Kit Number 192201-001 Not Applicable	00 00 00 00 00 00 00 00 00 00	00 00 00 00 00 00 00 00 00 00
75	4B	**PRODUCT VERSION NUMBER** Type/Length (0C2h) Type = "ASCII+LATIN1" = (11)b length = 2 bytes = (000010)b	194	C2

COMMUNICATION BUS DESCRIPTIONS

DS450DC-3 series FRU (EEPROM) Data:

OFFSET		DEFINITION	SPEC VALUE	
(DEC)	(HEX)	(REMARKS)	(DEC)	(HEX)
		Product Version Number/Auto Rev		
76	4C	"0" = 30H	48	30
77	4D	"1" = 41H, SHOULD TRACK MODULE REVISION indicated on IPS	49	41
78	4E	**PRODUCT SERIAL NUMBER** Type/Length *PRODUCT SERIAL NUMBER IS BASED ON ASTEC SERIAL NUMBER FORMAT P/N: 417-00201000 7-6: (11)b, 8-bit ASCII + Latin1, 5-0: (001101)b, 13-byte allocation	205	CD
		PRODUCT SERIAL NUMBER Model ID		
79	4F	"G"= 47H	71	47
80	50	"2" = 32H	50	32
81	51	"6" = 36H	54	36
82	52	"8" = 38H	56	38
83	53	**MANUFACTURING YEAR AND WEEK CODE**	PER UNIT	
84	54	REFER TO 417-00201000 FOR DETAILS	PER UNIT	
85	55	**UNIQUE SERIAL NUMBER**	PER UNIT	
86	56	REFER TO 417-00201000 FOR DETAILS	PER UNIT	
87	57		PER UNIT	
88	58		PER UNIT	
		MODEL REVISION		
89	59	"0" = 30H	48	30
90	5A	"1" = 41H	49	41
91	5B	**MANUFACTURING LOCATION** "P" = 50H	80	50
92	5C	**ASSET TAG (0C8H)** 7-6: (11)b, 8-bit ASCII + Latin 1, 5-0: (001000)b, 8-byte allocation	200	C8
93	5D	NO ASSET TAG	0	00
94	5E		0	00
95	5F		0	00
96	60		0	00
97	61		0	00
98	62		0	00
99	63		0	00
100	64		0	00
101	65	**FRU FILE (0CFH)** 7-6: (11)b, 8-bit ASCII + Latin 1, 5-0: (001111)b, 15-byte allocation	207	CF
102	60	"D" = 44H	68	44
103	61	"S" = 53H	83	53
104	62	"4" = 34H	52	34
105	63	"5" = 35H	53	35
106	64	"0" = 30H	48	30
107	65	"D" = 44H	68	44
108	66	"C" = 43H	67	43
109	67	"-" = 2DH	45	2D
110	68	"3" = 33H	51	33
111	69	"-" = 5FH	95	5F
112	70	"R" = 52H	82	52
113	71	"E" = 45H	69	45
114	72	"V" = 56H	86	56
115	73	"0" = 30H	48	30
116	74	"1" = 41H	49	41
117	75	**END OF FIELDS MARKER (0C1H)**	193	C1
118	76	**RESERVED**	00	00

COMMUNICATION BUS DESCRIPTIONS

DS450DC-3 series FRU (EEPROM) Data:

OFFSET		DEFINITION	SPEC VALUE	
(DEC)	(HEX)	(REMARKS)	(DEC)	(HEX)
119	77	**ZERO CHECK SUM** [100H-((SUM OF BYTES 28H-76H) AND FFH)]	PER UNIT	
		MULTI RECORD AREA, 72 BYTES POWER SUPPLY RECORD HEADER		
120	78	**RECORD TYPE** (0x00 = Power Supply Information)	00	00
121	79	7:7 - End of List, (0)b 6:4 - Reserved, write as (000)b 3:0 - Record Format Version (0010)b = 2H	02	02
122	7A	**RECORD LENGTH** (24 Bytes)	24	18
123	7B	**RECORD CHECKSUM** (Zero Checksum from 7DH-94H)	136	88
124	7C	**HEADER CHECKSUM** (Zero Checksum from 78H-7BH)	94	5E
		POWER SUPPLY RECORD		
125 126	7D 7E	**Overall Capacity of the Power Supply** 15-12: (0000)b, reserved 11-0: (001000100110)b, 450W = 01C2H Stored with LSB first then MSB	176 4	C2 01
127 128	7F 80	**Peak VA** 15-12: (0000)b, reserved 11-0: NO PEAK VA RATING Stored with LSB first then MSB	00 00	00 00
129	81	**Inrush Current** (Amps) 21.0A=15H	21	15
130	82	**Inrush Interval** (ms), 00ms=00H	00	00
131 132	83 84	**Low End Input Voltage Range 1 (10mV)** 36V = 3600(*10mV) = 0E10H Stored with LSB first then MSB	16 14	10 0E
133 134	85 86	**High End Input Voltage Range 1 (10mV)** 75V =7500(*10mV) = 1D4CH Stored with LSB first then MSB	76 29	4C 1D
135 136	87 88	**Low End Input Voltage Range 2 (10mV)** (Only one input range) Stored with LSB first then MSB	00 00	00 00
137 138	89 8A	**High End Input Voltage Range 2 (10mV)** (Only one input range) Stored with LSB first then MSB	00 00	00 00
139	8B	**Low End Input Frequency Range,** 00Hz = 00H	00	00
140	8C	**High End Input Frequency Range,** 00Hz = 00H	00	00
141	8D	**D/C DROPOUT Tolerance** (ms), 1ms = 01H	01	01
142	8E	**Binary Flags** Bits 7-5: RESERVED Bit 4: (1)b, Tachometer Pulses Per Rotation / Predictive Fail Polarity [2 pulses per rotation = 1; 1 pulse per rotation = 0] or [Signal Asserted (1) Indicates Failure = 0, Signal De-asserted (0) Indicates Failure = 1] Bit 3: (1)b, Hot Swap / Redundancy Support Bit 2: (0)b, Auto Switch Support Bit 1: (0)b, Power Factor Correction Support Bit 0: (0)b, Predictive Fail Support	24	18
143 144	8F 90	**Peak Wattage Capacity and Holdup Time** Bits 15-12: Holdup Time in Seconds = 00H Bits 11-0: (000000000000)b, Peak Capacity in Watts = 00H	0 0	00 00
145 146 147	91 92 93	**Combined Wattage,** Not Applicable	0 0 0	00 00 00
148	94	**Predictive Fail Tachometer Lower Threshold,** not applicable.	0	00

COMMUNICATION BUS DESCRIPTIONS

DS450DC-3 series FRU (EEPROM) Data:

OFFSET		DEFINITION	SPEC VALUE	
(DEC)	(HEX)	(REMARKS)	(DEC)	(HEX)
12V DC OUTPUT RECORD HEADER				
149	95	**Record type ID** (0x01 = DC Output)	01	01
150	96	**End of List / Record Format Version Number** 7:7 - End of List, (0)b 6:4 - Reserved, write as (000)b 3:0 - Record Format Version, (0010)b = 2H	02	02
151	97	**RECORD LENGTH** (13 Bytes)	13	0D
152	98	**RECORD CHECKSUM** (Zero Checksum from 9AH to A6H)	233	E9
153	99	**HEADER CHECKSUM** (Zero Checksum from 95H to 98H)	07	07
12V OUTPUT RECORD				
154	9A	**+12V Output Information** Bit 7: Standby, (0)b Bits 6-4: Reserved, write as (000)b Bits 3-0: Output Number, (0001)b = 1H	1	01
155 156	9B 9C	**Nominal Voltage** 12.00V = 1200 (x10mV) = 04B0H Stored with LSB first then MSB	176 4	B0 04
157 158	9B 9C	**Maximum Negative Voltage Deviation** 11.64V = 1164 (x10mV) = 048CH Stored with LSB first then MSB	140 4	8C 04
159 160	9F A0	**Maximum Positive Voltage Deviation** 12.36V = 1236 (x10mV) = 04D4H Stored with LSB first then MSB	212 04	D4 04
161 162	A1 A2	**Ripple and Noise pk-pk 10Hz-30MHz (mV)** 120mV = 0078H Stored with LSB first then MSB	120 00	78 00
163 164	A3 A4	**Minimum Current Draw (10mA)** 0.00A = 0000 (x10mA) = 0000H Stored with LSB first then MSB	00 00	00 00
165 166	A5 A6	**Maximum Current Draw (10mA)** 37.00A = 3700 (x10mA) = E74H Stored with LSB first then MSB	116 014	74 0E
3V3VSB OUTPUT RECORD HEADER				
167	A7	**RECORD TYPE ID** (0x01 = DC Output)	01	01
168	A8	**End of List / Record Format Version Number** 7:7 - End of List, (0)b 6:4 - Reserved, write as (000)b 3:0 - Record Format Version, (0010)b = 2H	02	02
169	A9	**Record Length** (20 Bytes)	20	14
170	AA	**Record CHECKSUM** (Zero Checksum from ACH to BFH)	12	0C
171	AB	**Header CHECKSUM** (Zero Checksum from A7H to AAH)	221	DD
3V3VSB DC OUTPUT RECORD				
172	AC	**3V3SB Output Information,** 002 = 02H 7:7 - Standby, (1)b 6:4 - Reserved, write as (000)b 3:0 - Output Number, (0010)b = 2H	130	82
173 174	AD AE	**Nominal Voltage** 3.30V = 330 (x10mV) = 014AH Stored with LSB first then MSB	74 1	4A 01
175 176	AF B0	**Maximum Negative Voltage Deviation (10mV)** 3.20V = 320 (x10mV) = 0140H Stored with LSB first then MSB	64 1	40 01

COMMUNICATION BUS DESCRIPTIONS

DS450DC-3 series FRU (EEPROM) Data:

OFFSET		DEFINITION	SPEC VALUE	
(DEC)	(HEX)	(REMARKS)	(DEC)	(HEX)
177 178	B1 B2	**Maximum Positive Voltage Deviation** 3.40V = 340 (x10mV) = 0154H Stored with LSB first then MSB	84 1	54 01
179 180	B3 B4	**Ripple and Noise pk-pk 10Hz-30MHz(mV)** 100mV = 0064H Stored with LSB first then MSB	100 0	64 00
181 182	B5 B6	**Minimum Current Draw (10mA)** 0.00A = 0000 (x10mA) = 0000H Stored with LSB first then MSB	0 0	00 00
183 184	87 B8	**Maximum Current Draw (10mA)** 3.00A = 300 (x10mA) = 012CH Stored with LSB first then MSB	44 1	2C 01
185	B9	Reserved	0	00
186	BA	Reserved	0	00
187	BB	Reserved	0	00
188	BC	Reserved	0	00
189	BD	Reserved	0	00
190	BE	Reserved	0	00
191	BF	Reserved	0	00
192	C0	**FORMAT VERSION NUMBER** (Internal Use Area) 7:4 - Reserved, write as 0000b 3:0 - Format Version Number = 1H for this specification	1	01
193	C1		0	00
194	C2		0	00
195	C3		0	00
196	C4		0	00
197	C5		0	00
198	C6		0	00
199	C7		0	00
200	C8		0	00
201	C9		0	00
202	CA		0	00
203	CB		0	00
204	CC		0	00
205	CD		0	00
206	CE		0	00
207	CF		0	00
208	D0		0	00
209	D1		0	00
210	D2		0	00
211	D3		0	00
212	D4		0	00
213	D5		0	00
214	D6		0	00
215	D7		0	00
216	D8		0	00
217	D9		0	00
218	DA		0	00
219	DB		0	00
220	DC		0	00
221	DD		0	00
222	DE		0	00
223	DF		0	00
224	E0		0	00
225	E1		0	00
226	E2		0	00

COMMUNICATION BUS DESCRIPTIONS

DS450DC-3 series FRU (EEPROM) Data:

OFFSET		DEFINITION	SPEC VALUE	
(DEC)	(HEX)	(REMARKS)	(DEC)	(HEX)
227	E3		0	00
228	E4		0	00
229	E5		0	00
230	E6		0	00
231	E7		0	00
232	E8		0	00
233	E9		0	00
234	EA		0	00
235	EB		0	00
236	EC		0	00
237	ED		0	00
238	EE		0	00
239	EF		0	00
240	F0		0	00
241	F1		0	00
242	F2		0	00
243	F3		0	00
244	F4		0	00
245	F5		0	00
246	F6		0	00
247	F7		0	00
248	F8		0	00
249	F9		0	00
250	FA		0	00
251	FB		0	00
252	FC		0	00
253	FD		0	00
254	FE		0	00
255	FF	**Zero Check Sum** (Chassis Info) [100H-((Sum of bytes C0H-FEH) AND FFH)]	255	FF

COMMUNICATION BUS DESCRIPTIONS

FRU (EEPROM) Data

The FRU (Field Replaceable Unit) data format is compliant with the Intel IPMI v1.0 specification. The DS450DC-3-401 uses 1 page of EEPROM for FRU purpose. The one page of EEPROM contains up to 256 byte-sized data locations.

Where: OFFSET -The OFFSET denotes the address in decimal format of a particular data byte within DS450DC-3-401 EEPROM.

VALUE -The VALUE details data written to a particular memory location of the EEPROM.

DEFINITION -The contents DEFINITION refers to the definition of a particular data byte.

DS450DC-3-401 series FRU (EEPROM) Data:

OFFSET		DEFINITION	SPEC VALUE	
(DEC)	(HEX)	(REMARKS)	(DEC)	(HEX)
		COMMON HEADER, 8 BYTES		
0	00	**FORMAT VERSION NUMBER** (Common Header) 7:4 - Reserved, write as 0000b 3:0 - Format Version Number = 1h for this specification	0	00
1	01	**INTERNAL USE AREA OFFSET** (In multiples of 8 bytes)	1	01
2	02	**CHASSIS INFO AREA OFFSET** (In multiples of 8 bytes)	2	02
3	03	**BOARD INFO AREA OFFSET** (In multiples of 8 bytes)	3	03
4	04	**PRODUCT INFO AREA OFFSET** (In multiples of 8 bytes)	4	04
5	05	**MULTI RECORD AREA OFFSET** (In multiples of 8 bytes)	5	05
6	06	**PAD** write as 00h	6	06
7	07	**ZERO CHECK SUM** [100H-((Sum of bytes 00H-06H) AND FFH)]	7	07
		CHASSIS INFO AREA (32 BYTES)		
8	08	**FORMAT VERSION NUMBER** 7:4 - Reserved, write as 0000b 3:0 - Format Version Number = 1h for this specification	1	01
9	09	**CHASSIS INFO AREA LENGTH** (In multiple of 8 bytes)	4	04
10	0A	**CHASSIS TYPE**	0	00
11	0B	**CHASSIS PART NUMBER** Type/Length 10-byte allocation Type = “ASCII+LATIN1” = (11)b Length = 10 bytes = (001010)b	202	CA
12	0C	**CHASSIS PART NUMBER BYTES** (Default value is 0.)	0	00
13	0D		0	00
14	0E		0	00
15	0F		0	00
16	10		0	00
17	11		0	00
18	12		0	00
19	13		0	00
20	14		0	00
21	15		0	00
22	16	**CHASSIS SERIAL NUMBER Type/Length** 15-byte allocation	207	CF
		CHASSIS SERIAL NUMBER BYTES		
23	17	“D” = 44H	0	00
24	18	“S” = 53H	0	00
25	19	“4” = 34H	0	00
26	1A	“5” = 35H	0	00
27	1B	“0” = 30H	0	00
28	1C	“-” = 2DH	0	00
29	1D	“3” = 33H	0	00
30	1E	“-” = 2DH	0	00
31	1F	“4”= 34H	0	00
32	20	“-” = 2DH	0	00

COMMUNICATION BUS DESCRIPTIONS

DS450DC-3-401 series FRU (EEPROM) Data:

OFFSET		DEFINITION	SPEC VALUE	
(DEC)	(HEX)	(REMARKS)	(DEC)	(HEX)
33 34 35 36 37	21 22 23 24 25	“4” = 34H “0” = 30H “1” = 31H “R” = 52H “1” = 31H	52 48 49 82 49	34 30 31 52 31
38	26	End Tag	193	C1
39	27	**ZERO CHECK SUM** (100H-((Sum of byte 08h-26h) and FFH)	69	45
PRODUCT INFORMATION AREA, 80 BYTES				
40	28	**FORMAT VERSION NUMBER** (Product Info Area) 7:4 - Reserved, write as 0000b 3:0 - Format Version Number = 1h for this specification	1	01
41	29	**PRODUCT INFO AREA LENGTH** (In multiples of 8 bytes)	10	0A
42	2A	**Language Code (English = 19H)**	25	19
43	2B	**MANUFACTURER NAME TYPE/LENGTH** (0C5H) 7-6: (11)b, 8-bit ASCII + Latin 1, 5-0: (000101)b, 5-byte allocation	197	C5
		MANUFACTURER'S NAME		
44 45 46 47 48	2C 2D 2E 2F 30	“A” = 41h “S” = 53h “T” = 54h “E” = 45h “C” = 43h	65 83 84 69 67	41 53 54 45 43
49	31	**PRODUCT NAME** Type/Length (0CEH) 7-6: (11)b, 8-bit ASCII + Latin 1, 5-0: (001110)b, 14-byte allocation	202	CA
		PRODUCT NAME		
50 51 52 53 54 55 56 57 58 59	32 33 34 35 36 37 38 39 3A 3B	“D” = 44H “S” = 53H “4” = 34H “5” = 35H “0” = 30H “D” = 44H “C” = 43H “-” = 2DH “3” = 33H “ “ = 20H	68 83 52 53 48 68 67 45 51 32	44 53 34 35 30 44 43 2D 33 20
60	3C	**PRODUCT PART/MODEL NUMBER** Type/Length (0CAH) 7-6: (11)b, 8-bit ASCII + Latin 1, 5-0: (001010)b, 10-byte allocation	206	CE
		POWER SUPPLY CUSTOMER NUMBER		
61 62 63 64 65 66 67 68 69 70 71 72 73 74	3D 3E 3F 40 41 42 43 44 45 46 47 48 49 4A	“B” = 42H “G” = 47H “R” = 52H “0” = 30H “0” = 30H “3” = 33H “0” = 30H “3” = 33H “ “ = 20H “R” = 52H “A” = 41H “0” = 30H “0” = 30H “ “ = 20H	66 71 82 48 48 51 48 51 32 82 65 48 48 32	42 47 52 30 30 33 30 33 20 52 41 30 30 20
75	4B	**PRODUCT VERSION NUMBER** Type/Length (0C2h) Type = “ASCII+LATIN1” = (11)b length = 2 bytes = (000010)b	194	C2

COMMUNICATION BUS DESCRIPTIONS

DS450DC-3-401 series FRU (EEPROM) Data:

OFFSET		DEFINITION	SPEC VALUE	
(DEC)	(HEX)	(REMARKS)	(DEC)	(HEX)
		Product Version Number/Auto Rev		
76	4C	"0" = 30H	48	30
77	4D	"1" = 41H, SHOULD TRACK MODULE REVISION indicated on IPS	49	41
78	4E	**PRODUCT SERIAL NUMBER** Type/Length *PRODUCT SERIAL NUMBER IS BASED ON ASTEC SERIAL NUMBER FORMAT P/N: 417-00201000 7-6: (11)b, 8-bit ASCII + Latin1, 5-0: (001101)b, 13-byte allocation	205	CD
		PRODUCT SERIAL NUMBER Model ID		
79	4F	"I" = 49H	73	49
80	50	"6" = 36H	54	36
81	51	"1" = 31H	49	31
82	52	"5" = 35H	53	35
83	53	**MANUFACTURING YEAR AND WEEK CODE**	PER UNIT	
84	54	REFER TO 417-00201000 FOR DETAILS	PER UNIT	
85	55	**UNIQUE SERIAL NUMBER**	PER UNIT	
86	56	REFER TO 417-00201000 FOR DETAILS	PER UNIT	
87	57		PER UNIT	
88	58		PER UNIT	
		MODEL REVISION		
89	59	"0" = 30H	48	30
90	5A	"1" = 31H *SHOULD TRACK MODEL REVISION indicated on IPS	49	41
91	5B	**PRODUCT SERIAL NUMBER: MANUFACTURING LOCATION** "P" = 50H (P for Laguna, Philippines)	80	50
92	5C	**ASSET TAG (0C8H)** 7-6: (11)b, 8-bit ASCII + Latin 1, 5-0: (001000)b, 8-byte allocation	200	C8
93	5D	NO ASSET TAG	0	00
94	5E		0	00
95	5F		0	00
96	60		0	00
97	61		0	00
98	62		0	00
99	63		0	00
100	64		0	00
101	65	**FRU FILE (0CFH)** 7-6: (11)b, 8-bit ASCII + Latin 1, 5-0: (001111)b, 15-byte allocation	207	CF
102	60	"D" = 44H	68	44
103	61	"S" = 53H	83	53
104	62	"4" = 34H	52	34
105	63	"5" = 35H	53	35
106	64	"0" = 30H	48	30
107	65	"D" = 44H	68	44
108	66	"C" = 43H	67	43
109	67	"-" = 2DH	45	2D
110	68	"3" = 33H	51	33
111	69	"-" = 5FH	95	5F
112	70	"R" = 52H	82	52
113	71	"E" = 45H	69	45
114	72	"V" = 56H	86	56
115	73	"0" = 30H	48	30
116	74	"1" = 41H	49	41
117	75	**END OF FIELDS MARKER (0C1H)**	193	C1
118	76	**RESERVED**	00	00

COMMUNICATION BUS DESCRIPTIONS

DS450DC-3-401 series FRU (EEPROM) Data:

OFFSET		DEFINITION	SPEC VALUE	
(DEC)	(HEX)	(REMARKS)	(DEC)	(HEX)
119	77	**ZERO CHECK SUM** [100H-((SUM OF BYTES 28H-76H) AND FFH)]	PER UNIT	
		MULTI RECORD AREA, 72 BYTES **POWER SUPPLY RECORD HEADER**		
120	78	**RECORD TYPE** (0x00 = Power Supply Information)	00	00
121	79	7:7 - End of List, (0)b 6:4 - Reserved, write as (000)b 3:0 - Record Format Version (0010)b = 2H	02	02
122	7A	**RECORD LENGTH** (24 Bytes)	24	18
123	7B	**RECORD CHECKSUM** (Zero Checksum from 7DH-94H)	136	88
124	7C	**HEADER CHECKSUM** (Zero Checksum from 78H-7BH)	94	5E
		POWER SUPPLY RECORD		
125 126	7D 7E	**Overall Capacity of the Power Supply** 15-12: (0000)b, reserved 11-0: (001000100110)b, 450W = 01C2H Stored with LSB first then MSB	194 1	C2 01
127 128	7F 80	**Peak VA** 15-12: (0000)b, reserved 11-0: NO PEAK VA RATING Stored with LSB first then MSB	00 00	00 00
129	81	**Inrush Current** (Amps) 21.0A=15H	21	15
130	82	**Inrush Interval** (ms), 00ms=00H	00	00
131 132	83 84	**Low End Input Voltage Range 1 (10mV)** 36V = 3600(*10mV) = 0E10H Stored with LSB first then MSB	16 14	10 0E
133 134	85 86	**High End Input Voltage Range 1 (10mV)** 75V = 7500(*10mV) = 1D4CH Stored with LSB first then MSB	76 29	4C 1D
135 136	87 88	**Low End Input Voltage Range 2 (10mV)** (Only one input range) Stored with LSB first then MSB	00 00	00 00
137 138	89 8A	**High End Input Voltage Range 2 (10mV)** (Only one input range) Stored with LSB first then MSB	00 00	00 00
139	8B	**Low End Input Frequency Range,** 00Hz = 00H	00	00
140	8C	**High End Input Frequency Range,** 00Hz = 00H	00	00
141	8D	**D/C DROPOUT Tolerance** (ms), 1ms = 01H	01	01
142	8E	**Binary Flags** Bits 7-5: RESERVED Bit 4: (1)b, Tachometer Pulses Per Rotation / Predictive Fail Polarity [2 pulses per rotation = 1; 1 pulse per rotation = 0] or [Signal Asserted (1) Indicates Failure = 0, Signal De-asserted (0) Indicates Failure = 1] Bit 3: (1)b, Hot Swap / Redundancy Support Bit 2: (0)b, Auto Switch Support Bit 1: (0)b, Power Factor Correction Support Bit 0: (0)b, Predictive Fail Support	24	18
143 144	8F 90	**Peak Wattage Capacity and Holdup Time** Bits 15-12: Holdup Time in Seconds = 00H Bits 11-0: (000000000000)b, Peak Capacity in Watts = 00H	0 0	00 00
145 146 147	91 92 93	**Combined Wattage,** Not Applicable	0 0 0	00 00 00
148	94	**Predictive Fail Tachometer Lower Threshold,** not applicable.	0	00

COMMUNICATION BUS DESCRIPTIONS

DS450DC-3-401 series FRU (EEPROM) Data:

OFFSET		DEFINITION	SPEC VALUE	
(DEC)	(HEX)	(REMARKS)	(DEC)	(HEX)
12V DC OUTPUT RECORD HEADER				
149	95	**Record type ID** (0x01 = DC Output)	01	01
150	96	**End of List / Record Format Version Number** 7:7 - End of List, (0)b 6:4 - Reserved, write as (000)b 3:0 - Record Format Version, (0010)b = 2H	02	02
151	97	**RECORD LENGTH** (13 Bytes)	13	0D
152	98	**RECORD CHECKSUM** (Zero Checksum from 9AH to A6H)	233	E9
153	99	**HEADER CHECKSUM** (Zero Checksum from 95H to 98H)	07	07
12V OUTPUT RECORD				
154	9A	**+12V Output Information** Bit 7: Standby, (0)b Bits 6-4: Reserved, write as (000)b Bits 3-0: Output Number, (0001)b = 1H	1	01
155 156	9B 9C	**Nominal Voltage** 12.00V = 1200 (x10mV) = 04B0H Stored with LSB first then MSB	176 4	B0 04
157 158	9B 9C	**Maximum Negative Voltage Deviation** 11.64V = 1164 (x10mV) = 048CH Stored with LSB first then MSB	140 4	8C 04
159 160	9F A0	**Maximum Positive Voltage Deviation** 12.36V = 1236 (x10mV) = 04D4H Stored with LSB first then MSB	212 04	D4 04
161 162	A1 A2	**Ripple and Noise pk-pk 10Hz-30MHz (mV)** 120mV = 0078H Stored with LSB first then MSB	120 00	78 00
163 164	A3 A4	**Minimum Current Draw (10mA)** 0.00A = 0000 (x10mA) = 0000H Stored with LSB first then MSB	00 00	00 00
165 166	A5 A6	**Maximum Current Draw (10mA)** 37.00A = 3700 (x10mA) = E74H Stored with LSB first then MSB	116 014	74 0E
3V3VSB OUTPUT RECORD HEADER				
167	A7	**RECORD TYPE ID** (0x01 = DC Output)	01	01
168	A8	**End of List / Record Format Version Number** 7:7 - End of List, (0)b 6:4 - Reserved, write as (000)b 3:0 - Record Format Version, (0010)b = 2H	02	02
169	A9	**Record Length** (20 Bytes)	20	14
170	AA	**Record CHECKSUM** (Zero Checksum from ACH to BFH)	12	0C
171	AB	**Header CHECKSUM** (Zero Checksum from A7H to AAH)	221	DD
3V3VSB DC OUTPUT RECORD				
172	AC	**3V3SB Output Information,** 002 = 02H 7:7 - Standby, (1)b 6:4 - Reserved, write as (000)b 3:0 - Output Number, (0010)b = 2H	130	82
173 174	AD AE	**Nominal Voltage** 3.30V = 330 (x10mV) = 014AH Stored with LSB first then MSB	74 1	4A 01
175 176	AF B0	**Maximum Negative Voltage Deviation (10mV)** 3.20V = 320 (x10mV) = 0140H Stored with LSB first then MSB	64 1	40 01

COMMUNICATION BUS DESCRIPTIONS

DS450DC-3-401 series FRU (EEPROM) Data:

OFFSET		DEFINITION	SPEC VALUE	
(DEC)	(HEX)	(REMARKS)	(DEC)	(HEX)
177 178	B1 B2	**Maximum Positive Voltage Deviation** 3.40V = 340 (x10mV) = 0154H Stored with LSB first then MSB	84 1	54 01
179 180	B3 B4	**Ripple and Noise pk-pk 10Hz-30MHz(mV)** 100mV = 0064H Stored with LSB first then MSB	100 0	64 00
181 182	B5 B6	**Minimum Current Draw (10mA)** 0.00A = 0000 (x10mA) = 0000H Stored with LSB first then MSB	0 0	00 00
183 184	87 B8	**Maximum Current Draw (10mA)** 3.00A = 300 (x10mA) = 012CH Stored with LSB first then MSB	44 1	2C 01
185	B9	Reserved	0	00
186	BA	Reserved	0	00
187	BB	Reserved	0	00
188	BC	Reserved	0	00
189	BD	Reserved	0	00
190	BE	Reserved	0	00
191	BF	Reserved	0	00
192	C0	**FORMAT VERSION NUMBER** (Internal Use Area) 7:4 - Reserved, write as 0000b 3:0 - Format Version Number = 1H for this specification	1	01
193	C1		0	00
194	C2		0	00
195	C3		0	00
196	C4		0	00
197	C5		0	00
198	C6		0	00
199	C7		0	00
200	C8		0	00
201	C9		0	00
202	CA		0	00
203	CB		0	00
204	CC		0	00
205	CD		0	00
206	CE		0	00
207	CF		0	00
208	D0		0	00
209	D1		0	00
210	D2		0	00
211	D3		0	00
212	D4		0	00
213	D5		0	00
214	D6		0	00
215	D7		0	00
216	D8		0	00
217	D9		0	00
218	DA		0	00
219	DB		0	00
220	DC		0	00
221	DD		0	00
222	DE		0	00
223	DF		0	00
224	E0		0	00
225	E1		0	00
226	E2		0	00

COMMUNICATION BUS DESCRIPTIONS

DS450DC-3-401 series FRU (EEPROM) Data:

OFFSET		DEFINITION	SPEC VALUE	
(DEC)	(HEX)	(REMARKS)	(DEC)	(HEX)
227	E3		0	00
228	E4		0	00
229	E5		0	00
230	E6		0	00
231	E7		0	00
232	E8		0	00
233	E9		0	00
234	EA		0	00
235	EB		0	00
236	EC		0	00
237	ED		0	00
238	EE		0	00
239	EF		0	00
240	F0		0	00
241	F1		0	00
242	F2		0	00
243	F3		0	00
244	F4		0	00
245	F5		0	00
246	F6		0	00
247	F7		0	00
248	F8		0	00
249	F9		0	00
250	FA		0	00
251	FB		0	00
252	FC		0	00
253	FD		0	00
254	FE		0	00
255	FF	**Zero Check Sum** (Chassis Info) [100H-((Sum of bytes C0H-FEH) AND FFH)]	255	FF

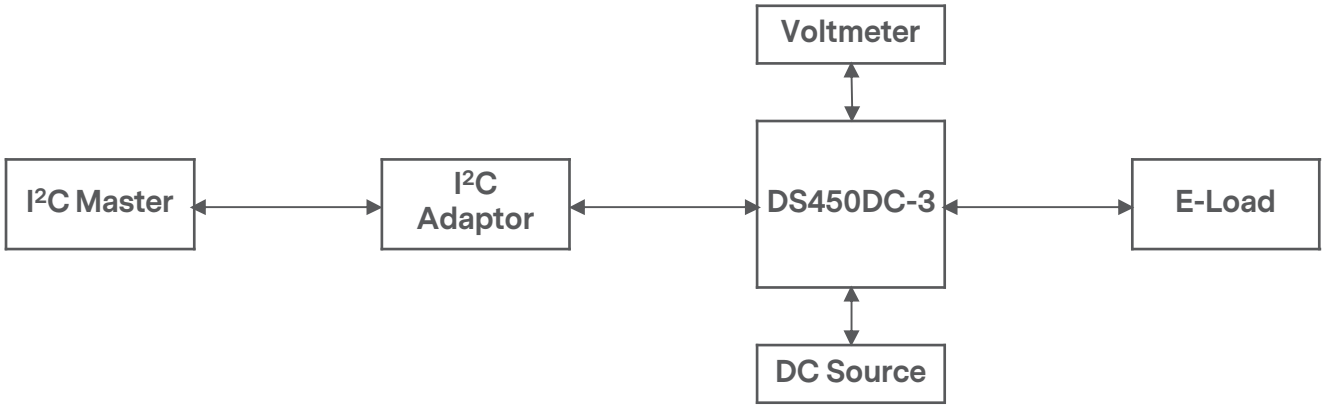
PMBus™ SPECIFICATIONS

The DS450DC-3 is compliant with the industry standard I²C protocol for monitoring and control of the power supply via the I²C interface port.

DS450DC-3 Series I²C General Instructions

Equipment Setup

The following is typical I²C communication setup:



APPLICATION NOTES

Current Sharing

The DS450DC-3 series' main output V1 is equipped with current sharing capability. This will allow up to 4 power supplies to be connected in parallel for higher power application. Current share accuracy is typically 10% of full load. When supplying light loads between 10% and 20% of its rated load, the power supplies will share within 20% accuracy. (Below 10% load, there is no guarantee of output current sharing). If any power supply is hot swapped, no glitch will occur that violates the regulation limits of the power supply defined in this specification.

Compute current share voltage using formula below:

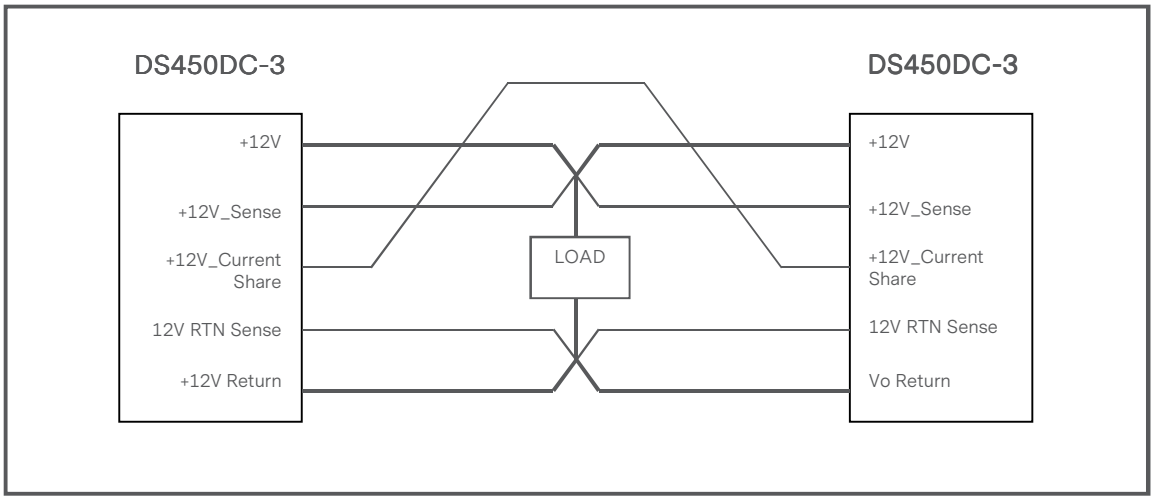
I Share bus voltage = (output current * 8.0V)/12V full load current.

Current share voltages computed by using above formula may not be accurate below 20-25% load due to non-linearity at lighter loads.

APPLICATION NOTES

Redundancy / Fault Tolerance

The DS450DC-3 series power supplies can be connected in the following to provide redundancy/fault tolerance operation:

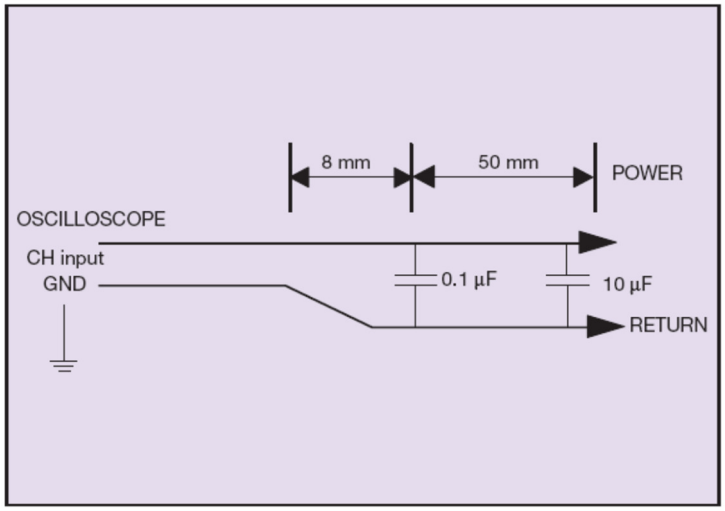


This will allow up to N* power supplies to be connected in an N+1 redundant load. Any failure of one power supply in parallel as well as hot swapping shall not cause more than a 5% (which ever is greater) change in any output. Current share accuracy is typically 10% of full load. The failure of one or more supplies will not cause the remaining supplies to violate any of the input or output specifications noted in this specification including all status signals.

APPLICATION NOTES

Output Ripple and Noise Measurement

The setup outlined in the diagram below has been used for output voltage ripple and noise measurements on the DS450DC-3 series. When measuring output ripple and noise, a scope jack in parallel with a 0.1uF ceramic chip capacitor, and a 10uF tantalum capacitor will be used. Oscilloscope can be set to 20MHz bandwidth for this measurement.



RECORD OF REVISION AND CHANGES

Issue	Date	Description	Originators
1.2	09.26.2019	First issue	F. Hao
1.3	03.02.2021	Update cover and back cover	C. Liu
1.4	05.09.2022	Add UKCA Mark	C. Liu

ABOUT ADVANCED ENERGY

Advanced Energy (AE) has devoted more than three decades to perfecting power for its global customers. AE designs and manufactures highly engineered, precision power conversion, measurement and control solutions for mission-critical applications and processes.

Our products enable customer innovation in complex applications for a wide range of industries including semiconductor equipment, industrial, manufacturing, telecommunications, data center computing, and medical. With deep applications know-how and responsive service and support across the globe, we build collaborative partnerships to meet rapid technological developments, propel growth for our customers, and innovate the future of power.

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