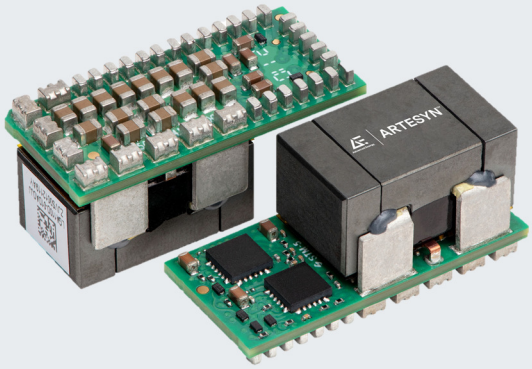
TECHNICAL REFERENCE NOTE

ARTESYN LGA110D SERIES

Non Isolated DCDC Converter



PRODUCT DESCRIPTION

The LGA110D power supply features a 7.5 to 14 Vdc input voltage range and a 350 W output power.

The LGA110D is a new design of high performance DC-DC converter. LGA110D has 2 phase design. It offers a total 350W output with dimensions 27.5 mm x 12.8 mm x 13.4 mm. State-of-the-art circuit topology provides a very high efficiency up to 96% which allows an operating temperature range of -40^{O}C to +85^{O}C.

Further features include remote On/Off, variable output voltage as well as over-current protection, over-voltage protection, and over-temperature protection.

AT A GLANCE

Total Power

350 Watts

Total Current

110 A (Single)

55 A (Dual)

Output Voltage

0.5 to 5 Vdc

# of Outputs

Dual or Single

RoHS

SPECIAL FEATURES

- 2 phase design
- Dual or single output configuration possible
- High efficiency up to 96%
- Small size 27.5 mm x 12.8 mm x 13.4 mm (LxWxH)
- PMBus™ supporting
- No minimum load requirement
- Wide operating temperature range
- Exceptional power density 203W/sq-in
- Automatic loop compensation
- Analogue or digital control
- Tape and reel packaging
- Reflow compatible
- Possible to stack up to 4 for 440 A
- Support 1 to 8 phase configuration up to 40 combinations with 1 to 4 modules
- I-mon and T-mon supported
- IPC9592B compliant

SAFETY

- Designed to meet EN62368

WARRANTY

- 2 years (consult factory for extended terms)

PATENT

Pending www.artesyn.com/ep-patents

Pending

artesyn.com/IP

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MODEL NUMBERS

Standard	Input Voltage	Output Voltage	Minimum Load	Maximum Load
LGA110D-01DADJJ	7.5 to 14 Vdc	0.5 to 5.0 Vdc	0 A	110 A

Order Information

LGA	110	D	-	01	D	ADJ		J
①	②	③		④	⑤	⑥	⑦	⑧

①	Model series	LGA: Series name
②	Output current	110: Rated output current = 110 A
③	Control	D: Digital control POL
④	Input voltage range	01: 7.5 to 14 Vdc
⑤	Number of outputs	D: Dual output
⑥	Output type	ADJ: Adjustable output
⑦	Other options	Blank: Latching mode during protection
⑧	RoHS compliance	J: Pb free (RoHS 6/6 compliant)

Options

None

ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings

Stress in excess of those listed in the "Absolute Maximum Ratings" may cause permanent damage to the power supply. These are stress ratings only and functional operation of the unit is not implied at these or any other conditions above those given in the operational sections of this TRN. Exposure to any absolute maximum rated condition for extended periods may adversely affect the power supply's reliability.

Table 1. Absolute Maximum Ratings

Parameter	Model	Symbol	Min	Typ	Max	Unit
Input Voltage (DC continuous operation)	All models	$V_{IN,DC}$	-	-	15	V
Operating Ambient Temperature[1]	All models	T_A	-40	-	+85	^{O}C
Storage Temperature	All models	T_{STG}	-40	-	+125	^{O}C
Output Voltage	All models	V_O	0.5	-	5.0	V
Logic I/O Voltage SHARE, EN1, EN2, PG1, PG2, SALRT, SCL, SDA, SYNC, VSET1, VSET2, CFG, ADDR, ASCRCFG	All models		-0.3	-	6.0	V
Analog Input Voltages VS1+, VS1-, VS2+, VS2-	All models		-0.3	-	6.0	V

Note 1 - At low temperatures (at < -20 degC), the accuracy of PMBus™ monitored parameters will be adversely affected. At high temperatures, please refer to "Thermal Derating" section.

ELECTRICAL SPECIFICATIONS

Input Specifications

Table 2. Input Specifications

Parameter	Condition[1]	Symbol	Min	Nom	Max	Unit
Operating Input Voltage, DC	$0.5 \le V_O \le 3.3$ V $0.5 \le V_O \le 5$ V	$V_{IN,DC}$	7.5 10	- -	14 14	V
Maximum Input Current		$I_{IN,max}$	-	-	40	A
Standby Input Current (V_O = Off, I_O = 0A, Enable OFF)	f_{SW} = 500 KHz	I_{IN}	-	60	65	mA
Standby Input Power (V_O = Off, I_O = 0A, Enable OFF)	f_{SW} = 500 KHz	P_{IN}	-	0.75	0.8	W
Operating Efficiency	V_{IN} = 12 V, T_A = 25°C 1.0 V at 110 A 1.8 V at 100 A 2.5 V at 90 A 3.3 V at 80 A 5.0 V at 70 A		 87.5 91.5 93.0 94.0 95.0	 88.5 92.5 94.0 95.0 96.0	 - - - - -	%
Input Capacitor (Internal)			-	140	-	uF
Input Capacitor (External required)[2]			-	88	-	uF
Input Voltage UVLO Threshold Range[3]	Falling Rising		6.5 -	6.9 7.2	- 7.5	V
Logic Input/Output Characteristics						
Logic Input Low, V_{IL}			-	-	0.8	V
Logic Input High, V_{IH}			2.05	-	-	V
Logic Output Low, V_{OL}	2 mA sinking		-	-	0.5	V
Logic Output High, V_{OH}	2 mA sourcing		4.25	-	-	V
Logic Input Leakage Current			-100	20	100	nA

Note 1 - Typical values given at V_{IN}=12 V, switching frequency = 500 KHz for 0.5 V ≤ V_O ≤ 5 V, T_A = 25°C, unless otherwise specified under conditions.
Note 2 - Minimum: 4 x 22 uF/16 V 0805 ceramic cap (C2012X6S1C226M125AC or equivalent)
Note 3 - For 5 V V_O configuration, it will use PMBus to set UVLO (Falling) to 8.9 V and UVLO (Rising) to 9.2 V.

ELECTRICAL SPECIFICATIONS

Output Specifications

Table 3. Output Specifications

Parameter	Condition	Symbol	Min	Nom	Max	Unit
Output Voltage	V_{IN} = 7.5 V to 14 V V_{IN} = 10 V to 14 V	V_O1, V_O2[1] V_O1, V_O2[1]	0.5 0.5	- -	3.3 5.0	Vdc Vdc
Output Current (Independent Output 1 and 2)	V_O1 or V_O2 = 0.5 V V_O1 or V_O2 = 1.0 V V_O1 or V_O2 = 1.8 V V_O1 or V_O2 = 2.5 V V_O1 or V_O2 = 3.3 V V_O1 or V_O2 = 5.0 V	I_O1, I_O2	0 0 0 0 0 0	- - - - - -	55 55 50 45 40 35	A
Output Current (Combined Output 1 and 2)	V_O = 0.5 V V_O = 1.0 V V_O = 1.8 V V_O = 2.5 V V_O = 3.3 V V_O = 5.0 V	I_O	0 0 0 0 0 0	- - - - - -	110 110 100 90 80 70	A
Output Power	All	P_O	-	-	350	W
Output Set-point Accuracy[2]	Set by PMBus or 1% trim resistors		-1.2	-	+1.2	%
Output Voltage Set-point Resolution	Set by PMBus command		-	±0.05	-	%
Output Voltage Positive Sensing Bias Current	VS [1,2] + = 4 V (negative = sinking)		0	-	30	µA
Output Voltage Negative Sensing Bias Current	VS [1,2] - = 0 V		-30	-	0	µA
Line Regulation	0.5 V ≤ V_O ≤ 1.0 V 1.0 V < V_O ≤ 5.0 V		- -	2 0.2	10 1	mV %
Load Regulation	0.5 V ≤ V_O ≤ 1.0 V 1.0 V < V_O ≤ 5.0 V		- -	5 0.5	10 1	mV %
Ripple and Noise Single Output[3]	0.5 V ≤ V_O ≤ 1.0 V 1.0 V < V_O ≤ 5.0 V		- -	10 1	20 2	mV %
Ripple and Noise Dual Outputs (V_O1, V_O2)[3]	0.5 V ≤ V_O ≤ 1.0 V 1.0 V < V_O ≤ 5.0 V		- -	10 1	20 2	mV %
Transient Response Deviation[3] (Independent Output 1 and 2)	50% of Io step load slew rate = 1 A/us 0.5 V ≤ V_O ≤ 1.0 V 1.0 V < V_O ≤ 5.0 V		- -	60 3	80 4	mV %
Transient Response Deviation[3] (Combined Output 1 and 2)	50% of I_O step load slew rate = 1A/us 0.5 V ≤ V_O ≤ 1.0 V 1.0 V < V_O ≤ 5.0 V		- -	30 3	40 4	mV %
Output Capacitor per Output[3] (external minimum)	Dual outputs Single output	C_O C_O	- -	1990 3980	- -	uF uF

Note 1 - V_O1 and V_O2 are the outputs of dual output module.
Note 2 - V_O measured at the termination of the VSx+ and VSx- sense points across line, load, temperature variation.
Note 3 - Dual mode (2 outputs): 2 x 680 uF/6.3 V Polymer Tan caps (T530X687M006ATE010 or equivalent)
+ 6 x 100 uF/6.3 V X6S 1210 ceramic caps (GRM32EC80J107ME20L or equivalent)
+ 3 x 10 uF/16 V X6S 0603 ceramic caps (GRM188C81C106MA73 or equivalent)
Single mode (1 output): 4 x 680 uF/6.3 V Polymer Tan caps (T530X687M006ATE010 or equivalent)
+ 12 x 100 uF/6.3 V X6S 1210 ceramic caps (GRM32EC80J107ME20L or equivalent)
+ 6 x 10 uF/16 V X6S 0603 ceramic caps (GRM188C81C106MA73 or equivalent)

ELECTRICAL SPECIFICATIONS

Output Specifications

Table 3. Output Specifications con't

Parameter	Condition	Symbol	Min	Nom	Max	Unit
Switching Frequency[4]	0.5 V ≤ V_O ≤ 5.0 V	f_{SW}	450	500	800	KHz
PMBus™ Clock Frequency[5]			-	400	-	KHz
Ton Delay/Toff Delay			-	0	-	mS
Ton Delay/Toff Delay Range	Set by PMBus command		0.1	-	125	mS
Ramp Delay/Toff Delay Accuracy	Turn on, Turn off delay		-300	-	300	uS
Ton Ramp/Toff Ramp Duration	Default (2-phase or 2 channels only)		-	3	10	mS
Power Good Vo Threshold			85	90	95	%
Power Good Vo Hysteresis			-	5	10	%
Power Good Delay Applies to turn on only (Low to High transition)	Factory default Set using PMBus		- 0	1 -	2 125	mS
Power Good Low Voltage	V_{IN} from 0 to 14 V		-	-	0.5	V
MTBF	Calculated according to Bellcore or Telcordia TR-NTW-000332 at 40°C full-load		50	-	-	MHours
Shelf Life	Calculated at 40°C		2	-	-	Years
Over Voltage Protection	All		-	115	-	%V_O
Over Current Protection[6]	I_O1, I_O2		-	65	-	A
Over Temperature Protection (at Mosfet)	All		-	125	-	°C

Note 4 - The switching frequency of single output or dual outputs must be the same. 500 KHz is the default frequency set in LGA110D module.
Note 5 - For operation PMBus™ clock frequency at 400 KHz, see PMBus™ Power System Management Protocol Specification for timing parameter limits.
Note 6 - The OCP set point applies per phase. The total OCP current value will be twice of I_O1 in single mode. Please refer to Table 7 for OCP setting.

ELECTRICAL SPECIFICATIONS

LGA110D-01DADJJ Performance Curves (Efficiency at different Vin)

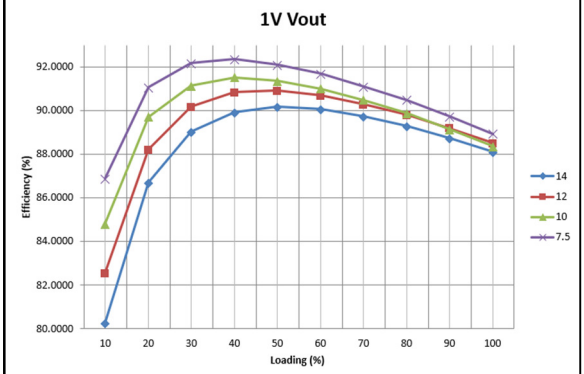


Figure 1: LGA110D-01DADJJ Efficiency Curves @ 25 degC

Loading: I_O = 10% increment to 110 A, V_O = 1 V f_{SW} = 500 KHz

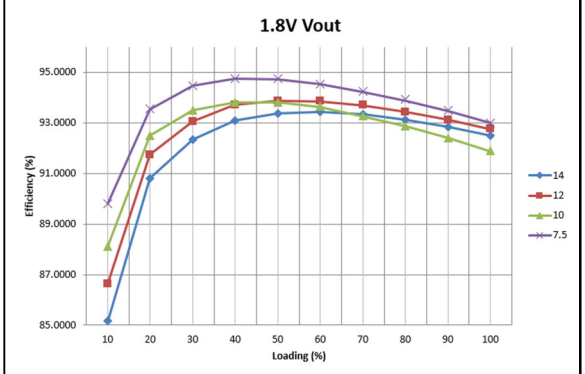


Figure 2: LGA110D-01DADJJ Efficiency Curves @ 25 degC

Loading: I_O = 10% increment to 100 A, V_O = 1.8 V f_{SW} = 500 KHz

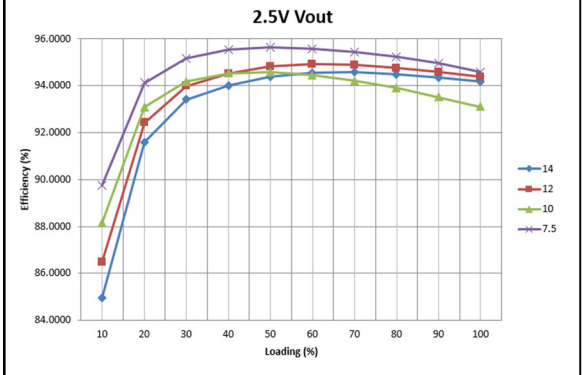


Figure 3: LGA110D-01DADJJ Efficiency Curves @ 25 degC

Loading: I_O = 10% increment to 90 A, V_O = 2.5 V f_{SW} = 500 KHz

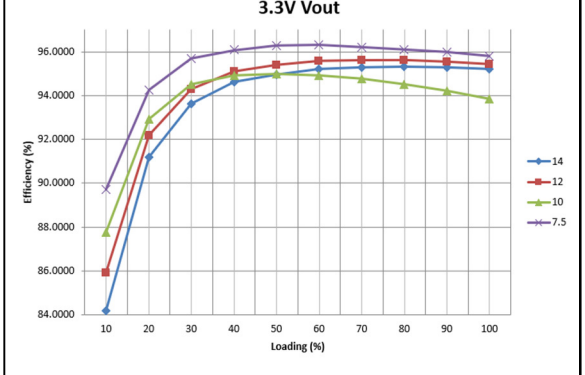


Figure 4: LGA110D-01DADJJ Efficiency Curves @ 25 degC

Loading: I_O = 10% increment to 80 A, V_O = 3.3 V f_{SW} = 500 KHz

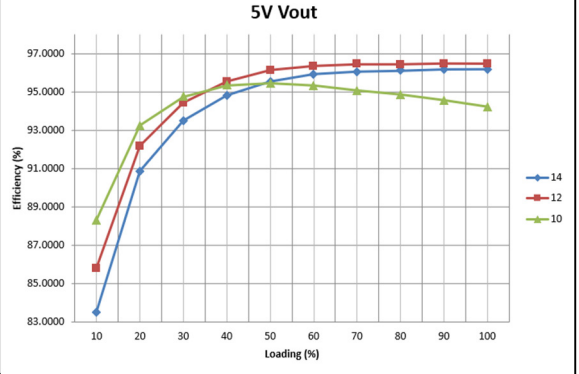


Figure 5: LGA110D-00DADJJ Efficiency Curves @ 25 degC

Loading: I_O = 10% increment to 70 A, V_O = 5 V f_{SW} = 500 KHz

ELECTRICAL SPECIFICATIONS

LGA110D-01DADJJ Performance Curves (Efficiency at different switching frequency)

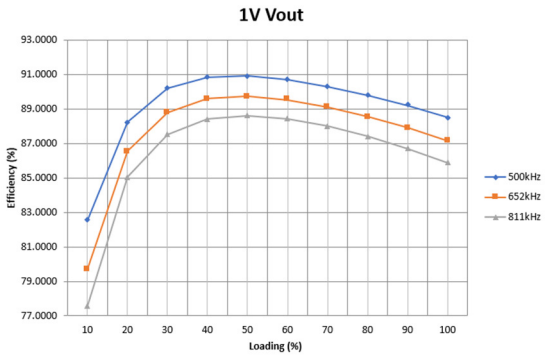


Figure 6: LGA110D-01DADJJ Efficiency Curves @ 25 degC

Loading: I_O = 10% increment to 110 A

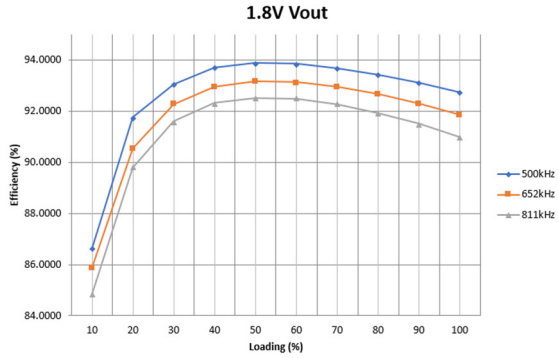


Figure 7: LGA110D-01DADJJ Efficiency Curves @ 25 degC

Loading: I_O = 10% increment to 100 A

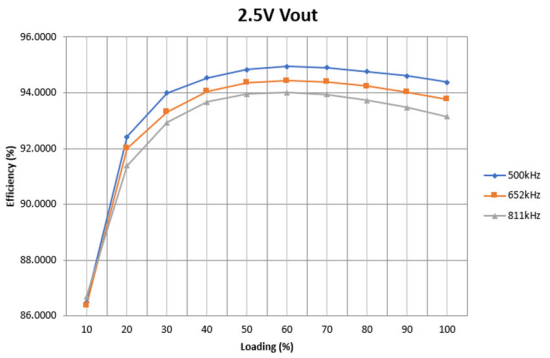


Figure 8: LGA110D-01DADJJ Efficiency Curves @ 25 degC

Loading: I_O = 10% increment to 90 A

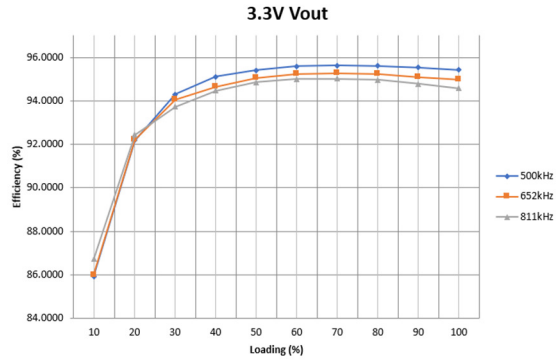


Figure 9: LGA110D-01DADJJ Efficiency Curves @ 25 degC

Loading: I_O = 10% increment to 80 A

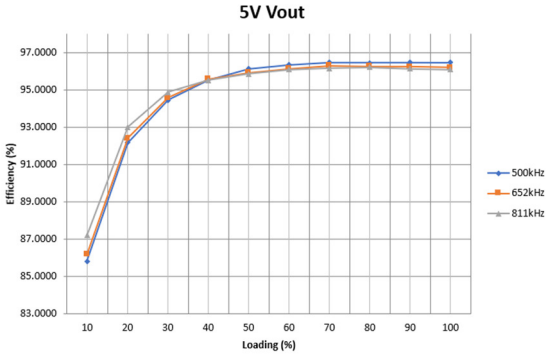


Figure 10: LGA110D-01DADJJ Efficiency Curves @ 25 degC

Loading: I_O = 10% increment to 70 A

ELECTRICAL SPECIFICATIONS

LGA110D-01DADJJ Performance Curves (Thermal derating)

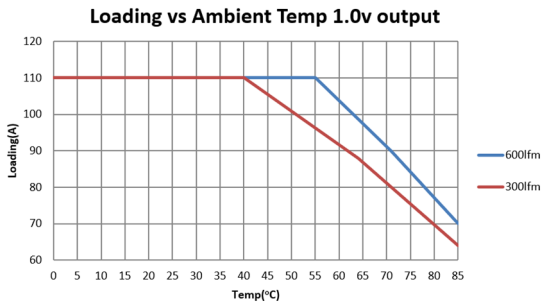


Figure 11: LGA110D-01DADJJ Thermal Derating Curves (Two modules with longitudinal airflow)
Vin= 12 V Load: I_O = 64 to 110 A, V_O = 1.0 V f_{SW} = 500 KHz

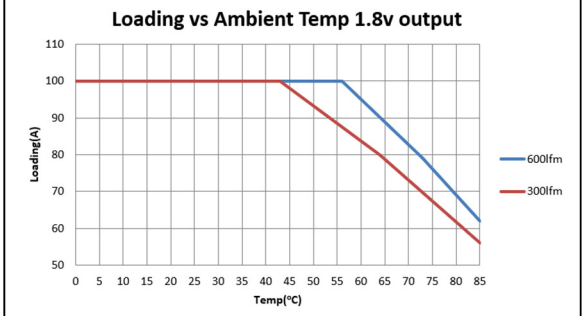


Figure 12: LGA110D-01DADJJ Thermal Derating Curves (Two modules with longitudinal airflow)
Vin= 12 V Load: I_O = 56 to 100 A, V_O = 1.8 V f_{SW} = 500 KHz

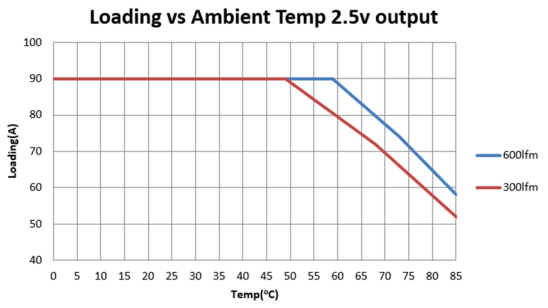


Figure 13: LGA110D-01DADJJ Thermal Derating Curves (Two modules with longitudinal airflow)
Vin= 12 V Load: I_O = 52 to 90 A, V_O = 2.5 V f_{SW} = 500 KHz

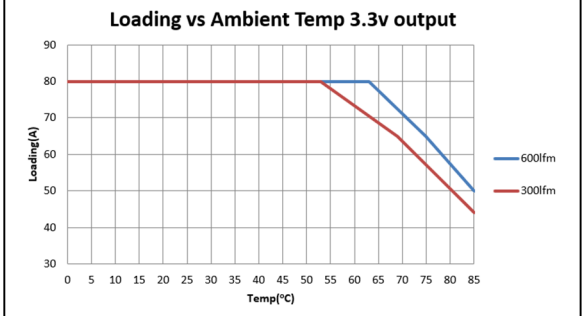


Figure 14: LGA110D-01DADJJ Thermal Derating Curves (Two modules with longitudinal airflow)
Vin= 12 V Load: I_O = 44 to 80 A, V_O = 3.3 V f_{SW} = 500 KHz

Note: One module temperature is much better than two modules.

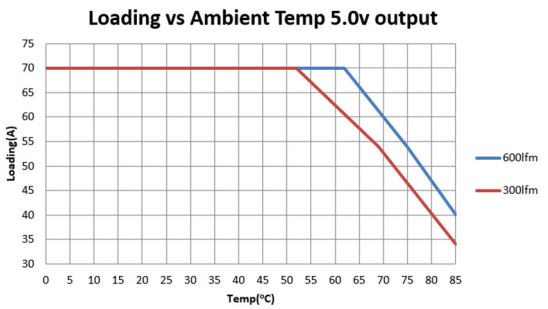


Figure 15: LGA110D-01DADJJ Thermal Derating Curves (Two modules with longitudinal airflow)
Vin= 12 V Load: I_O = 34 to 70 A, V_O = 5.0 V f_{SW} = 500 KHz

ELECTRICAL SPECIFICATIONS

LGA110D-01DADJJ Performance Curves (Output ripple)

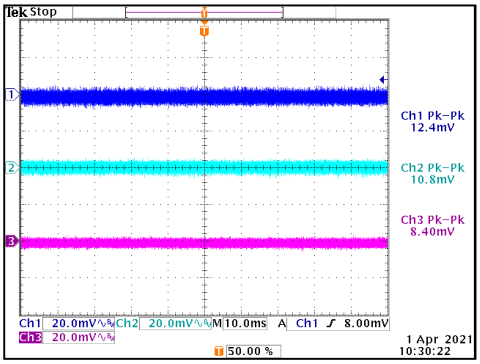


Figure 16: LGA110D-01DADJJ Ripple and Noise – V_O = 0.5 V
Full Load
Ch 1:V_O1 Ch 2: V_O2 Ch 3: V_O3

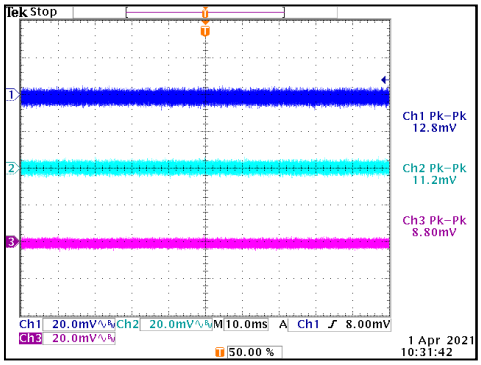


Figure 17: LGA110D-01DADJJ Ripple and Noise – V_O = 1.0 V
Full Load
Ch 1: V_O1 Ch 2: V_O2 Ch 3: V_O3

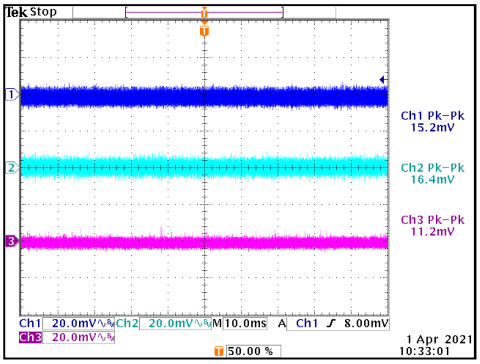


Figure 18: LGA110D-01DADJJ Ripple and Noise – V_O = 1.8 V
Full Load
Ch 1: V_O1 Ch 2: V_O2 Ch 3: V_O3

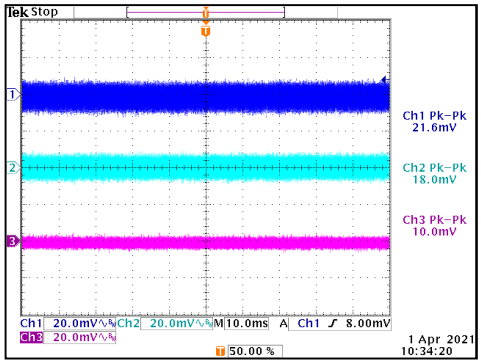


Figure 19: LGA110D-01DADJJ Ripple and Noise – V_O = 2.5 V
Full Load
Ch 1: V_O1 Ch 2: V_O2 Ch 3: V_O3

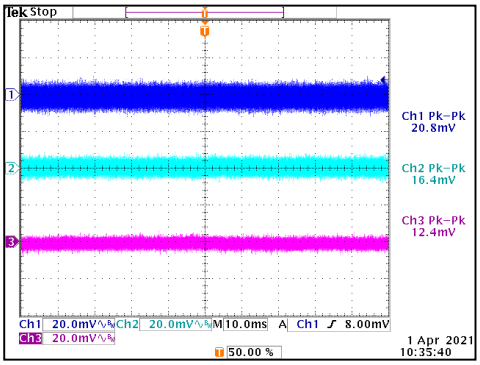


Figure 20: LGA110D-01DADJJ Ripple and Noise – V_O = 3.3 V
Full Load
Ch 1: V_O1 Ch 2: V_O2 Ch 3: V_O3

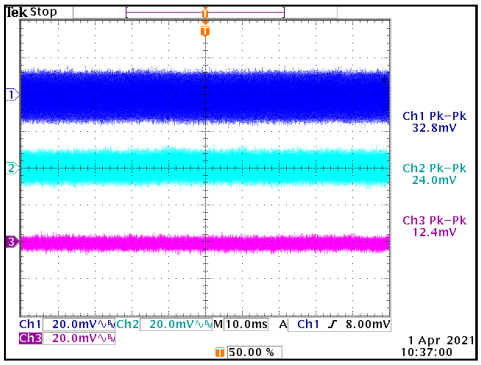


Figure 21: LGA110D-01DADJJ Ripple and Noise – V_O = 5.0 V
Full Load
Ch 1: V_O1 Ch 2: V_O2 Ch 3: V_O3

ELECTRICAL SPECIFICATIONS

LGA110D-01DADJJ Performance Curves (Start Up)

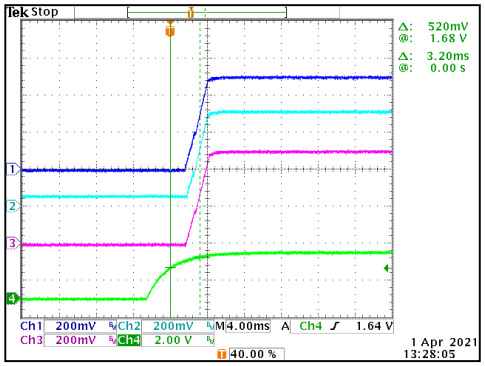


Figure 22: LGA110D-01DADJJ Start Up – V_O = 0.5 V
Full Load
Ch 1: V_O1 Ch 2: V_O2 Ch 3: V_O3 Ch 4: Enable

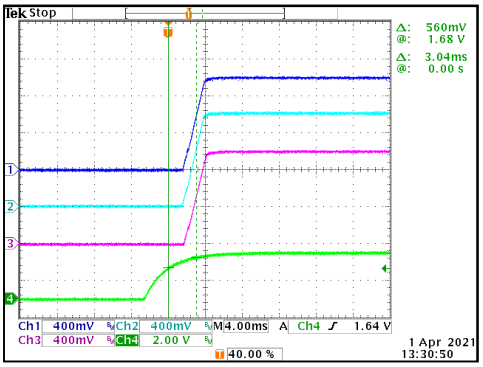


Figure 23: LGA110D-01DADJJ Start Up – V_O = 1 V
Full Load
Ch 1: V_O1 Ch 2: V_O2 Ch 3: V_O3 Ch 4: Enable

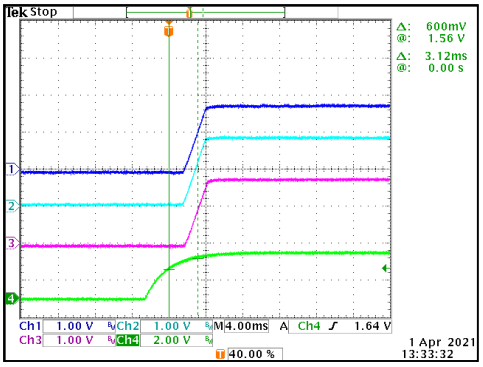


Figure 24: LGA110D-01DADJJ Start Up – V_O = 1.8 V
Full Load
Ch 1: V_O1 Ch 2: V_O2 Ch 3: V_O3 Ch 4: Enable

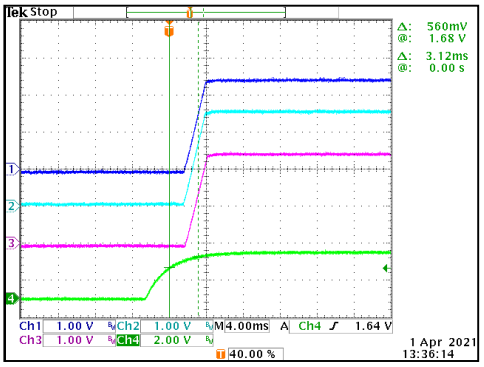


Figure 25: LGA110D-01DADJJ Start Up – V_O = 2.5 V
Full Load
Ch 1: V_O1 Ch 2: V_O2 Ch 3: V_O3 Ch 4: Enable

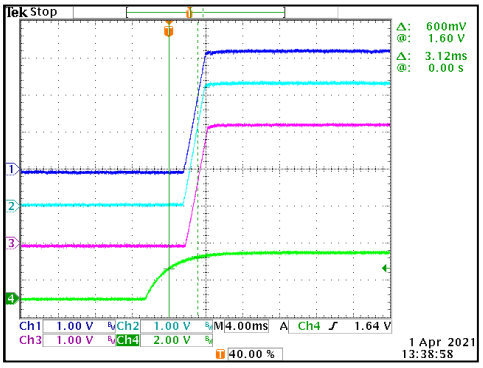


Figure 26: LGA110D-01DADJJ Start Up – V_O = 3.3 V
Full Load
Ch 1: V_O1 Ch 2: V_O2 Ch 3: V_O3 Ch 4: Enable

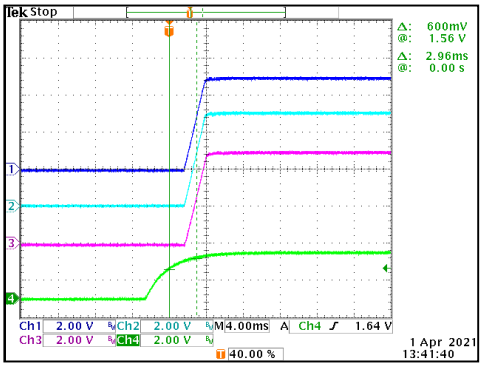


Figure 27: LGA110D-01DADJJ Start Up – V_O = 5.0 V
Full Load
Ch 1: V_O1 Ch 2: V_O2 Ch 3: V_O3 Ch 4: Enable

ELECTRICAL SPECIFICATIONS

LGA110D-01DADJJ Performance Curves (Slow dynamic load response – 2 phase 2 output)

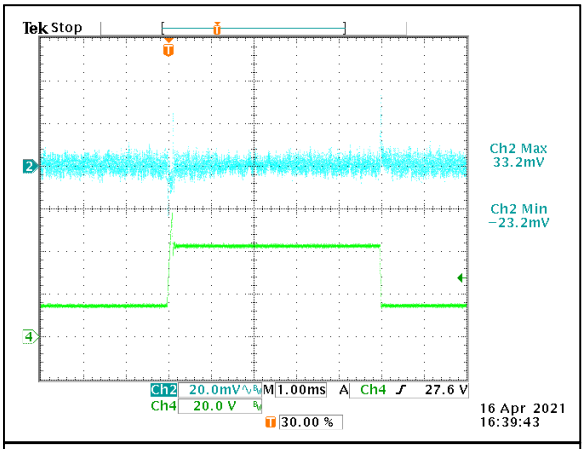


Figure 28: LGA110D-01DADJJ Transient Response – V_O Deviation
25% to 75% to 25% load change, 1 A/uS slew rate, V_{IN} = 12 Vdc V_O = 0.5 V
Ch 2: V_O Ch 4: I_O f_{SW} = 500KHz

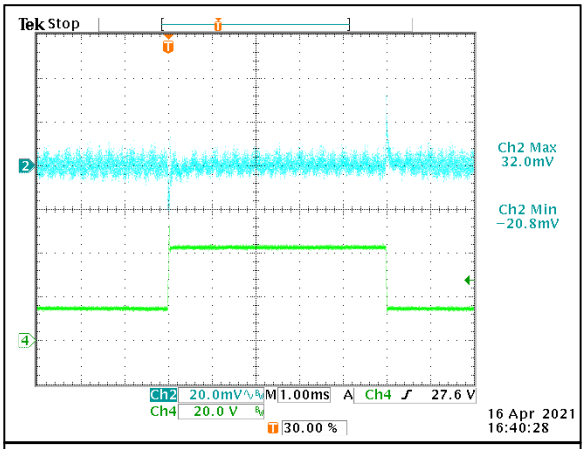


Figure 29: LGA110D-01DADJJ Transient Response – V_O Deviation
25% to 75% to 25% load change, 1 A/uS slew rate, V_{IN} = 12 Vdc V_O = 1.0 V
Ch 2: V_O Ch 4: I_O f_{SW} = 500KHz

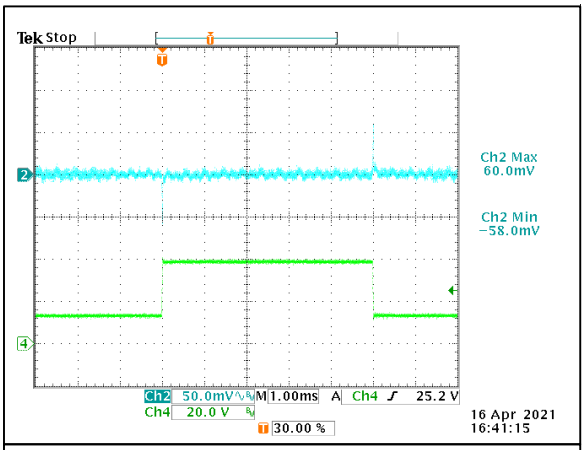


Figure 30: LGA110D-01DADJJ Transient Response – Vo Deviation
25% to 75% to 25% load change, 1 A/uS slew rate, V_{IN} = 12 Vdc V_O = 1.8 V
Ch 2: V_O Ch 4: I_O f_{SW} = 500KHz

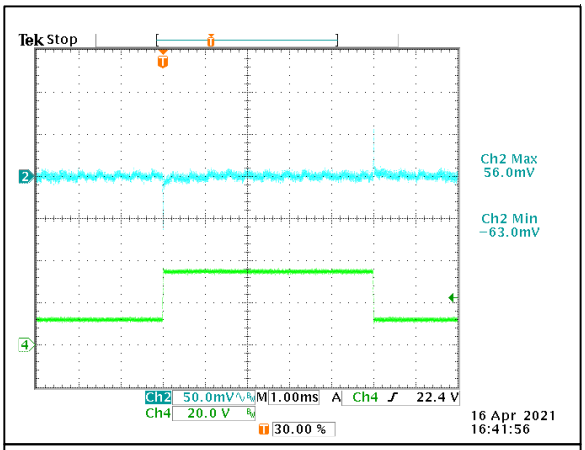


Figure 31: LGA110D-01DADJJ Transient Response – Vo Deviation
25% to 75% to 25% load change, 1 A/uS slew rate, V_{IN} = 12 Vdc V_O = 2.5 V
Ch 2: V_O Ch 4: I_O f_{SW} = 500KHz

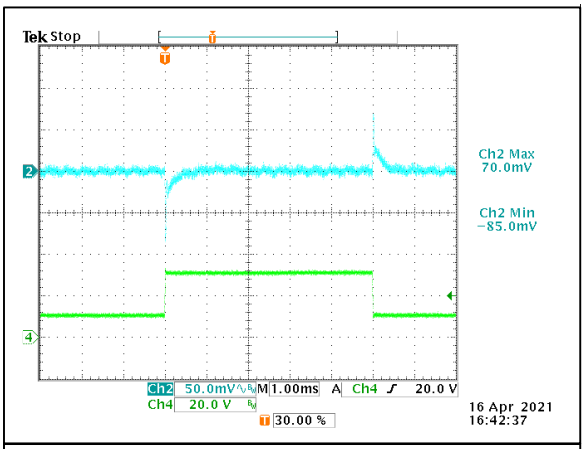


Figure 32: LGA110D-01DADJJ Transient Response – Vo Deviation
25% to 75% to 25% load change, 1 A/uS slew rate, V_{IN} = 12 Vdc V_O = 3.3 V
Ch 2: V_O Ch 4: I_O f_{SW} = 500KHz

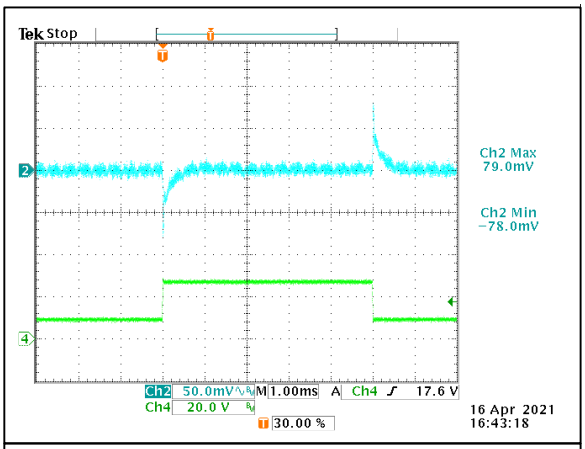


Figure 33: LGA110D-01DADJJ Transient Response – Vo Deviation
25% to 75% to 25% load change, 1 A/uS slew rate, V_{IN} = 12 Vdc V_O = 5.0 V
Ch 2: V_O Ch 4: I_O f_{SW} = 500KHz

ELECTRICAL SPECIFICATIONS

LGA110D-01DADJJ Performance Curves (Slow dynamic load response – 2 phase 1 output)

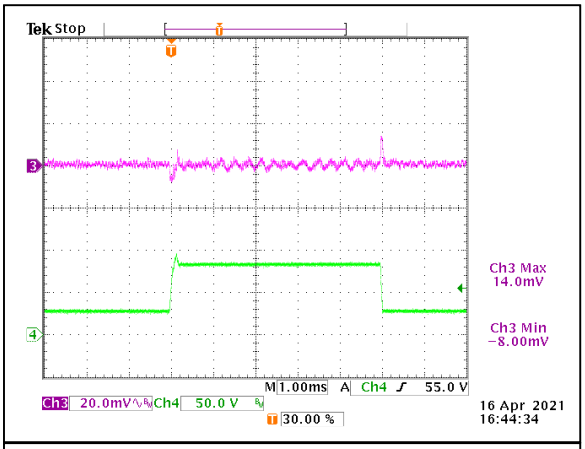


Figure 34: LGA110D-01DADJJ Transient Response – Vo Deviation
25% to 75% to 25% load change, 1 A/uS slew rate, V_{IN} = 12 Vdc V_O = 0.5 V
Ch 3: V_O Ch 4: I_O f_{SW} = 500 KHz

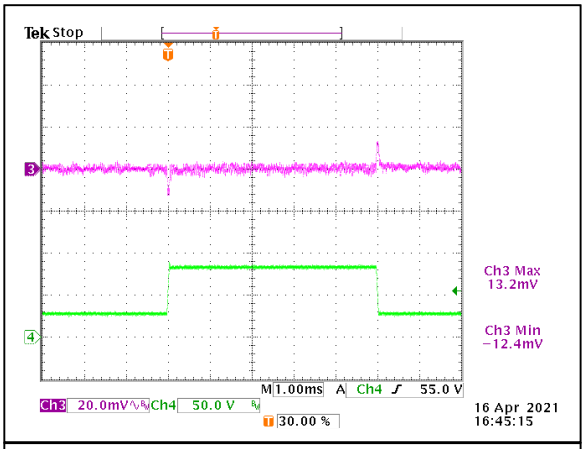


Figure 35: LGA110D-01DADJJ Transient Response – Vo Deviation
25% to 75% to 25% load change, 1 A/uS slew rate, V_{IN} = 12 Vdc V_O = 1.0 V
Ch 3: V_O Ch 4: I_O f_{SW} = 500 KHz

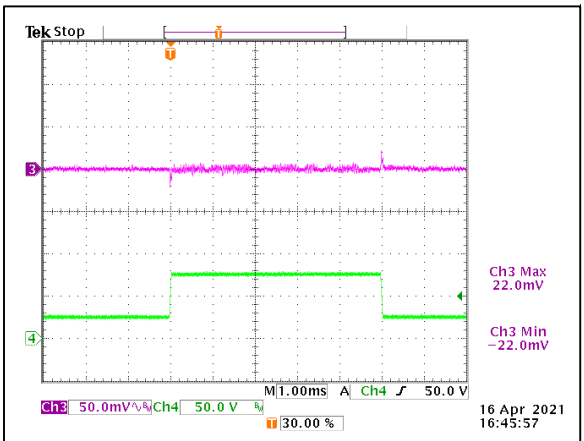


Figure 36: LGA110D-01DADJJ Transient Response – Vo Deviation
25% to 75% to 25% load change, 1 A/uS slew rate, V_{IN} = 12 Vdc V_O = 1.8 V
Ch 3: V_O Ch 4: I_O f_{SW} = 500 KHz

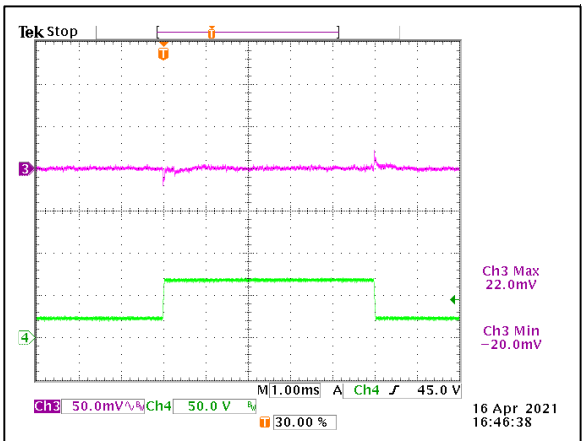


Figure 37: LGA110D-01DADJJ Transient Response – Vo Deviation
25% to 75% to 25% load change, 1 A/uS slew rate, V_{IN} = 12 Vdc V_O = 2.5 V
Ch 3: V_O Ch 4: I_O f_{SW} = 500 KHz

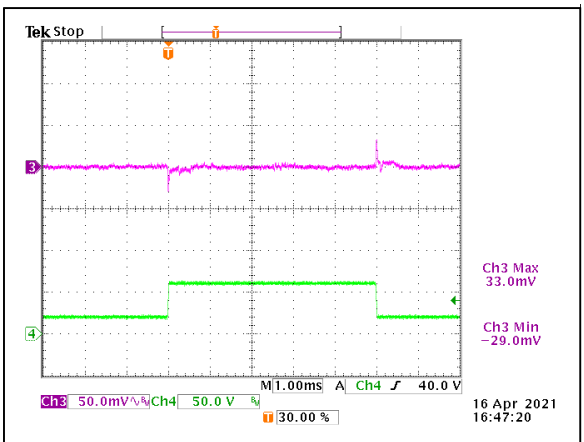


Figure 38: LGA110D-01DADJJ Transient Response – Vo Deviation
25% to 75% to 25% load change, 1 A/uS slew rate, V_{IN} = 12 Vdc V_O = 3.3 V
Ch 3: V_O Ch 4: I_O f_{SW} = 500 KHz

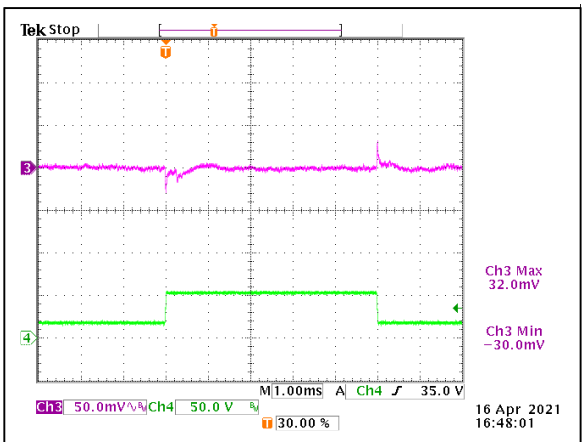


Figure 39: LGA110D-01DADJJ Transient Response – Vo Deviation
25% to 75% to 25% load change, 1 A/uS slew rate, V_{IN} = 12 Vdc V_O = 5.0 V
Ch 3: V_O Ch 4: I_O f_{SW} = 500 KHz

ELECTRICAL SPECIFICATIONS

LGA110D-01DADJJ Performance Curves (Fast dynamic load response – 2 phase 2 output)

Figure 40: LGA110D-01DADJJ Transient Response – Vo Deviation 25% to 75% to 25% load, 100 A/uS slew rate, V_{IN} = 12 Vdc V_O = 0.5 V
Ch 1: I_O Ch 2: V_O f_{SW} = 500 KHz

Figure 41: LGA110D-01DADJJ Transient Response – Vo Deviation 25% to 75% to 25% load, 100 A/uS slew rate, V_{IN} = 12 Vdc V_O = 1 V
Ch 1: I_O Ch 2: V_O f_{SW} = 500 KHz

LGA110D-01DADJJ Performance Curves (Fast dynamic load response – 2 phase 1 output)

Figure 42: LGA110D-01DADJJ Transient Response – Vo Deviation 25% to 75% to 25% load, 100 A/uS slew rate, V_{IN} = 12 Vdc V_O = 0.5 V
Ch 1: I_O Ch 2: V_O f_{SW} = 500 KHz

Figure 43: LGA110D-01DADJJ Transient Response – Vo Deviation 25% to 75% to 25% load, 100 A/uS slew rate, V_{IN} = 12 Vdc V_O = 1 V
Ch 1: I_O Ch 2: V_O f_{SW} = 500 KHz

ELECTRICAL SPECIFICATIONS

LGA110D-01DADJJ Performance Curves (Fast dynamic load response – 3 phase 1 output)

Figure 44: LGA110D-01DADJJ Transient Response – Vo Deviation 25% to 75% to 25% load, 100 A/uS slew rate, V_{IN} = 12 Vdc V_O = 0.5 V
Ch 1: I_O Ch 2: V_O f_{SW} = 500KHz

Figure 45: LGA110D-01DADJJ Transient Response – Vo Deviation 25% to 75% to 25% load, 100 A/uS slew rate, V_{IN} = 12 Vdc V_O = 1 V
Ch 1: I_O Ch 2: V_O f_{SW} = 500KHz

LGA110D-01DADJJ Performance Curves (Fast dynamic load response – 4 phase 1 output)

Figure 46: LGA110D-01DADJJ Transient Response – Vo Deviation 25% to 75% to 25% load, 100 A/uS slew rate, V_{IN} = 12 Vdc V_O = 0.5 V
Ch 1: I_O Ch 2: V_O f_{SW} = 500KHz

Figure 47: LGA110D-01DADJJ Transient Response – Vo Deviation 25% to 75% to 25% load, 100 A/uS slew rate, V_{IN} = 12 Vdc V_O = 1 V
Ch 1: I_O Ch 2: V_O f_{SW} = 500KHz

ELECTRICAL SPECIFICATIONS

Protection Function Specifications

Over Voltage Protection (OVP)

The LGA110D offers an internal output overvoltage protection circuit that can be used to protect sensitive load circuitry from being subjected to a voltage higher than its prescribed limits. A hardware comparator is used to compare the actual output voltage (seen at the VS pin) to a programmable threshold set to 15% higher than the target output voltage (the default setting).

If the VS voltage exceeds this threshold, the PG pin will de-assert and the module will latch.

Input Voltage Under Voltage Lock-Out Setting (UVLO)

The input under voltage lockout (UVLO) prevents the LGA110D from operating when the input falls below a preset threshold, indicating the input supply is out of its specified range. The input voltage under voltage lock-out threshold can be set between 0 V and 16 V using the VIN_UV_FAULT_LIMIT command. The default UVLO value is 6.7 V.

The default response from an under voltage fault is to shutdown and stay off until the fault has cleared and the module has been disabled and re-enabled.

When controlling the LGA110D exclusively through the PMBus™, a high voltage setting for UVLO can be used to prevent the LGA110D from being enabled until a lower voltage for UVLO is set using the VIN_UV_FAULT_LIMIT command.

Output Over Current Protection

The LGA110D can protect the power supply from damage from an overloaded or shorted output. Once the current trigger OCP set point, the unit will latch.

Over Temperature Protection

The LGA110D provide over temperature protection where the hotspot of the module. There are two over temperature protection sensing point, one is on the controller IC, the other one is on the Mosfet.

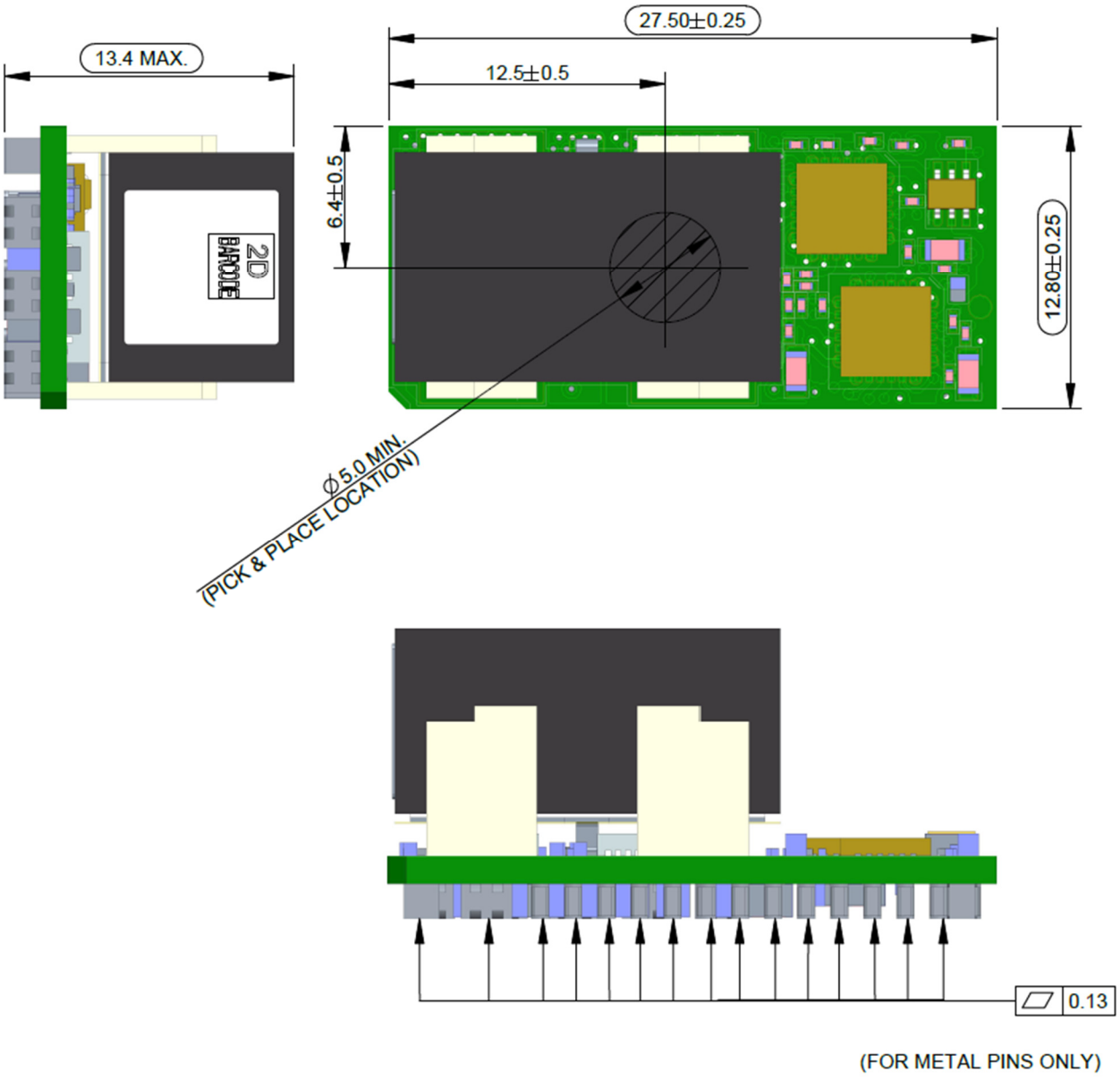
Once the module has been disabled due to over temperature fault, the unit will auto recover once temperature is below OT_WARN_LIMIT +110^{O}C.

MECHANICAL SPECIFICATIONS

Mechanical Drawing (Dimensioning and Mounting Locations)

Side view of standard metal-block pin termination type (LGA110D-01DADJJ)

Maximum Weight = 11.4 g



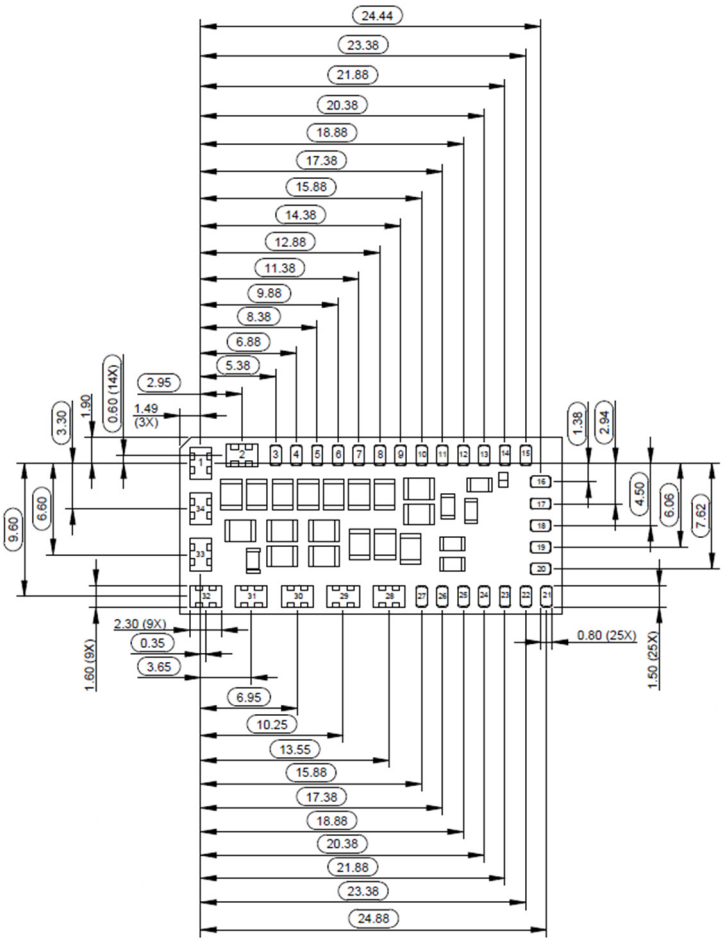
Notes: Dimensions are in millimeters.

MECHANICAL SPECIFICATIONS

Mechanical Drawing (Dimensioning and Mounting Locations)

Footprint Drawing of Metal Pins (Bottom View)

For standard metal-block pin termination (LGA110D-01DADJJ)



Notes: Dimensions are in millimeters.
Tolerance: Decimal .XX±0.25 mm
ANGLE ±1°

Table 4. Pin Assignments

Pin #	Function	Pin #	Function
1	Vin	18	SCL
2	GND	19	VSET/SA2
3	CFG1	20	SHARE2
4	ASCRCFG1	21	DDC2
5	CFG2	22	VS1-
6	ASCRCFG2	23	VS1+
7	VSET/SA1	24	SYNC
8	V1P51	25	PG2
9	SGND	26	VS2-
10	PG1	27	VS2+
11	EN1	28	V_O1
12	SALRT	29	V_O1
13	EN2	30	GND
14	SHARE1	31	V_O2
15	DDC1	32	V_O2
16	V1P52	33	GND
17	SDA	34	Vin

MECHANICAL SPECIFICATIONS

Mechanical Drawing (Dimensioning and Mounting Locations)

Recommended Pad Layout

For standard metal-block pin termination (LGA110D-01DADJJ)

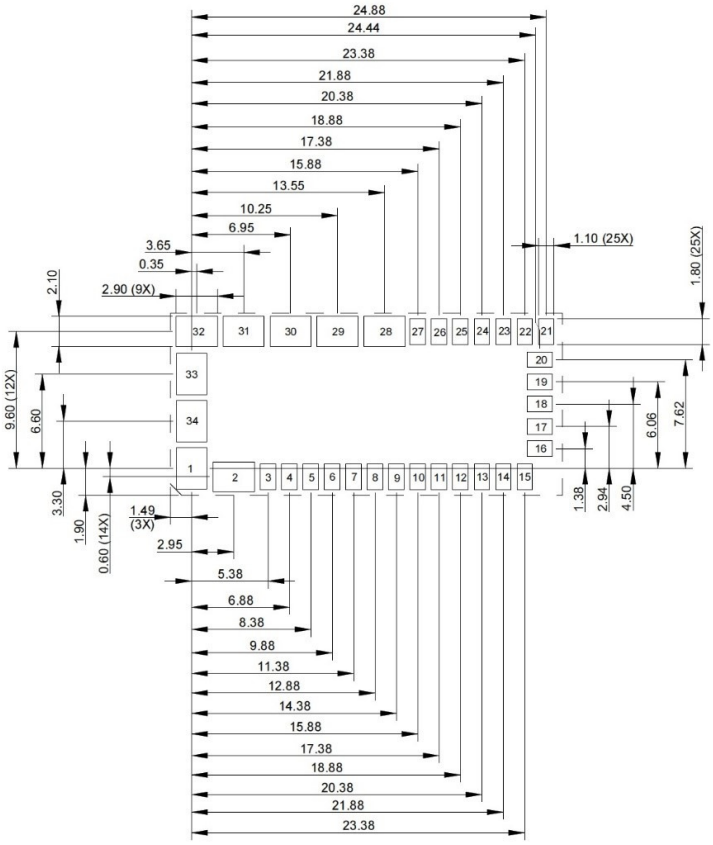


Table 4. Pin Assignments

Pin #	Function	Pin #	Function
1	Vin	18	SCL
2	GND	19	VSET/SA2
3	CFG1	20	SHARE2
4	ASCRCFG1	21	DDC2
5	CFG2	22	VS1-
6	ASCRCFG2	23	VS1+
7	VSET/SA1	24	SYNC
8	V1P51	25	PG2
9	SGND	26	VS2-
10	PG1	27	VS2+
11	EN1	28	V_O1
12	SALRT	29	V_O1
13	EN2	30	GND
14	SHARE1	31	V_O2
15	DDC1	32	V_O2
16	V1P52	33	GND
17	SDA	34	Vin

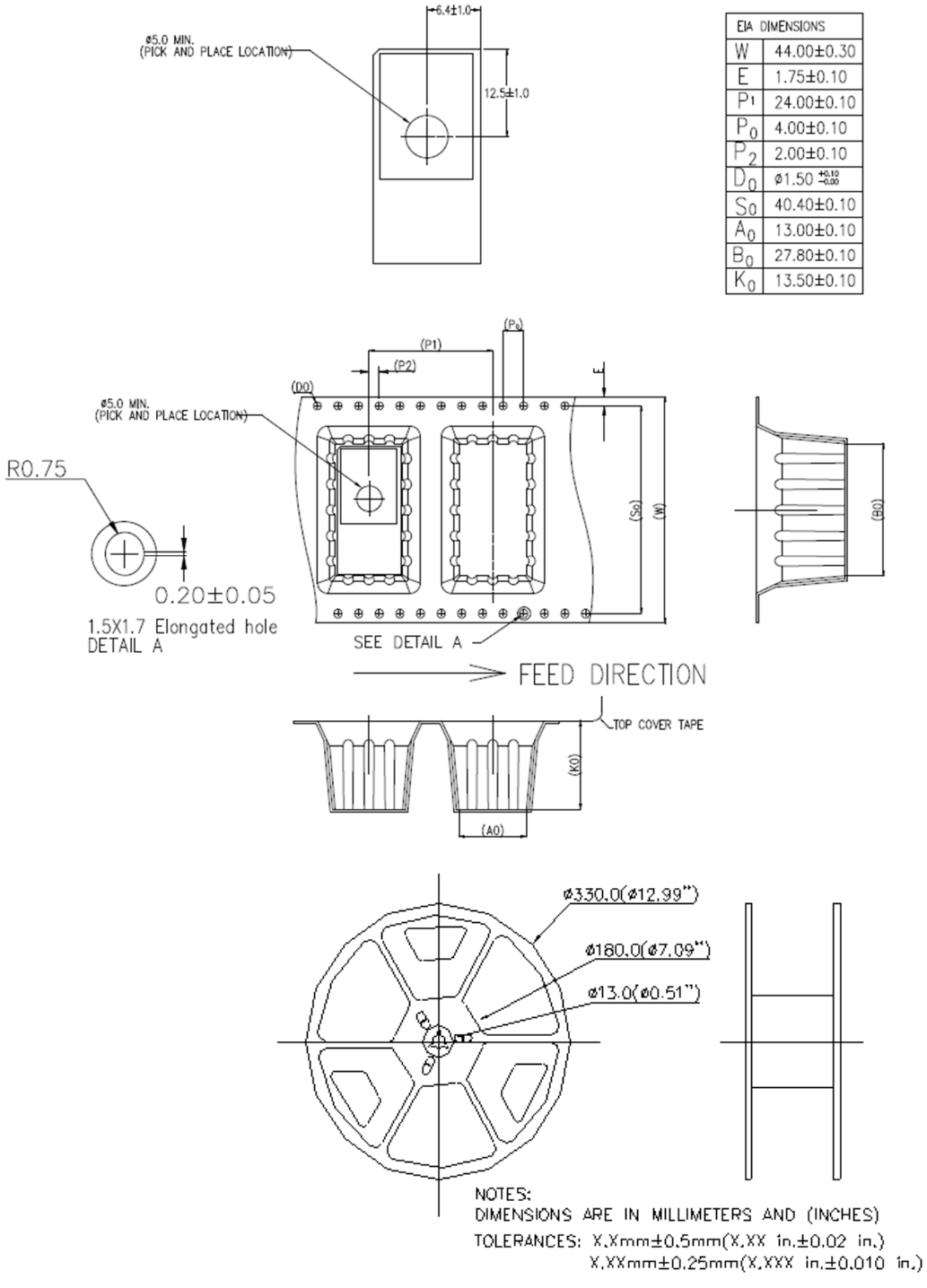
Notes: Dimensions are in millimeters.
Tolerance: Decimal .XX ± 0.15 mm
Dash line represents LGA110D module outline.

MECHANICAL SPECIFICATIONS

Mechanical Considerations

Surface Mount Tape & Reel

LGA110D-01DADJJ



EIA DIMENSIONS	
W	44.00±0.30
E	1.75±0.10
P_1	24.00±0.10
P_0	4.00±0.10
P_2	2.00±0.10
D_0	ø1.50 $^{+0.10}_{-0.00}$
S_0	40.40±0.10
A_0	13.00±0.10
B_0	27.80±0.10
K_0	13.50±0.10

MECHANICAL SPECIFICATIONS

Power and Control Signal Descriptions

Table 5. Power and Control Signal Descriptions

Pin #	Function	Type[1]	Control Pin
1	Vin	PWR	Input positive power pin.
2	GND	PWR	Power ground pin.
3	CFG1	M	V_O1 setting current sense, current limit and operating mode. Refer to configuration setting.
4	ASCRCFG1	M	V_O1 control loop configuration settings. Refer to control loop (ASCR) setting.
5	CFG2	M	V_O2 setting current sense, current limit and operating mode. Refer to configuration setting.
6	ASCRCFG2	M	V_O2 control loop configuration settings. Refer to control loop (ASCR) setting.
7	VSET/SA1	M	Assigns unique PMBus address for V_O1 and to set V_O1 set-point. See output voltage and address set section. Connect one resistor to SGND and a second resistor to V1P51. Default V_O1 maximum is 115% of VOUT setting, but this can be overridden with VOUT_MAX command using the PMBus interface.
8	V1P51	PWR	For VSET/SA1 pin-strap resistor setting only, not for external use.
9	SGND	PWR	Signal ground. SGND is shorted to GND internally on LGA110D.
10	PG1	O	V_O1 power-good output. Default is open drain.
11	EN1	I	Enable V_O1. Active signal enables.
12	SALRT	O	Serial alert. Connect to external host if desired. Requires a pull-up resistor to a 2.5 V to 5.5 V source, the source must be always on. 2.2 Kohm pull-up resistor is recommended.
13	EN2	I	Enable V_O2. Active signal enables.
14	SHARE1	I/O	SHARE Bus shall be connected together for multi-phase output configuration. Leave disconnected in single phase applications.
15	DDC1	I/O	DDC Bus shall be connected together for multi-phase output configuration. Leave disconnected in single phase applications.
16	V1P52	PWR	For VSET/SA2 pin-strap resistor setting only, not for external use.
17	SDA	I/O	Serial data. Connect to external host and/or to other LGA110D. Requires a pull-up resistor to a 2.5 V to 5.5 V source, the source must be always on. 2.2 Kohm pull-up resistor is recommended.
18	SCL	I/O	Serial clock. Connect to external host and/or to other LGA110D. Requires a pull-up resistor to a 2.5 V to 5.5 V source, the source must be always on. 2.2 Kohm pull-up resistor is recommended.
19	VSET/SA2	M	Assigns unique PMBus address for V_O2 and to set V_O2 set-point. See Output Voltage and Address set section. Connect one resistor to SGND and a second resistor to V1P52. Default Vo2 maximum is 115% of VOUT setting, but this can be overridden with VOUT_MAX command using the PMBus interface..
20	SHARE2	I/O	SHARE Bus shall be connected together for multi-phase output configuration. Leave disconnected in single phase applications.
21	DDC2	I/O	DDC Bus shall be connected together for multi-phase output configuration. Leave disconnected in single phase applications.
22	VS1-	I	Differential output V_O1 voltage sense feedback. Connect to negative output regulation point.
23	VS1+	I	Differential output V_O1 voltage sense feedback. Connect to positive output regulation point.

Note 1: I = Input, O = Output, PWR = Power or Ground, M = Multimode pins.

MECHANICAL SPECIFICATIONS

Power and Control Signal Descriptions

Table 5. Power and Control Signal Descriptions con't

Pin #	Function	Type[1]	Control Pin
24	SYNC	M/I/O	Clock synchronization pin. It's internal default to "Use internal clock and output internal clock" on V_O2 phase and "External clock" on V_O1 phase. V_O1 phase & V_O2 phase has been synchronized for 180^O phase shift internally. And 500KHz clock can be seen from the SYNC pin. For synchronization setting more than 1 module refer to Sync pin configuration on USER_CONFIG section. When used as part of a SYNC bus for phase spreading or current sharing, at most, one of the devices shall be configured to use this pin as output. All LGA110D modules are highly recommended to synchronize together. The "SYNC" pin can support synchronization up to 8 phases (or 4 modules).
25	PG2	O	V_O2 power-good output. Default is open drain.
26	VS2-	I	Differential output V_O2 voltage sense feedback. Connect to negative output regulation point.
27	VS2+	I	Differential output V_O2 voltage sense feedback. Connect to positive output regulation point.
28	V_O1	PWR	Output V_O1 positive power pin.
29	V_O1	PWR	Output V_O1 positive power pin.
30	GND	PWR	Power ground pin.
31	V_O2	PWR	Output V_O2 positive power pin.
32	V_O2	PWR	Output V_O2 positive power pin.
33	GND	PWR	Power ground pin.
34	Vin	PWR	Input positive power pin.

Note 1: I = Input, O = Output, PWR = Power or Ground, M = Multimode pins.

PMBUS™ SPECIFICATIONS

LGA110D PMBus™ Interface Support

PMBus™ Communications

The LGA110D provides a SMBus digital interface. The LGA110D can be used with any standard 2-wire SMBus host module. In addition, the module is compatible with SMBus version 2.0 and includes a SALRT line to help mitigate bandwidth limitations related to continuous fault monitoring. Pull-up resistors are required on the SMBus. The pull-up resistor may be tied to an external 3.3 V or 5 V supply as long as this voltage is present prior to or during module power-up. The ideal design will use a central pull-up resistor that is well-matched to the total load capacitance. The minimum pull-up resistance should be limited to a value that enables any module to assert the bus to a voltage that will ensure a logic 0 (typically 0.8 V at the module monitoring point) given the pull-up voltage and the pull-down current capability of the LGA110D. A pull-up resistor of 2.2 Kohm is a good value for most applications.

SMBus Data and Clock lines should be routed with a closely coupled return or ground plane to minimize coupled interference (noise). Excessive noise on the data and clock lines that cause the voltage on these lines to cross the high and low logic thresholds of 2.0 V and 0.8 V respectively will cause command transmissions to be interrupted and result in slow bus operation or missed commands. For less than 4 modules on a SMBus a 2.2 Kohm resistor on each line provides good performance.

The LGA110D accepts most standard PMBus™ commands. When enabling the module with ON_OFF_CONFIG command, it is recommended that the enable pin (EN1 and EN2) is tied to SGND.

In addition to bus noise considerations, it is important to ensure that user connections to the SMBus are compliant to the PMBus™ command standards. Any module that can malfunction in a way that permanently shorts SMBus lines will disable PMBus™ communications. Incomplete PMBus™ commands can also cause the LGA110D to halt PMBus™ communications. This can be corrected by disabling, then re-enabling the module. Highly recommend to have command validation after commands are set via PMBus communication.

Monitoring via PMBus™

A system controller can monitor a wide variety of different LGA110D parameters through the SMBus interface. The module can monitor for fault conditions by monitoring the SALRT pin, which will be asserted when any number of pre-configured fault conditions occur.

The module can also be monitored continuously for any number of power conversion parameters including but not limited to the following:

· Input voltage

· Output voltage

· Output current

· Internal junction temperature

· Fault status information

The PMBus™ Host should respond to SALRT as follows:

1. LGA110D module pulls SALRT Low.
2. PMBus™ Host detects that SALRT is low, performs transmission with Alert Response Address to find which LGA110D module is pulling SALRT low.
3. PMBus™ Host talks to the LGA110D module that has pulled SALRT low.

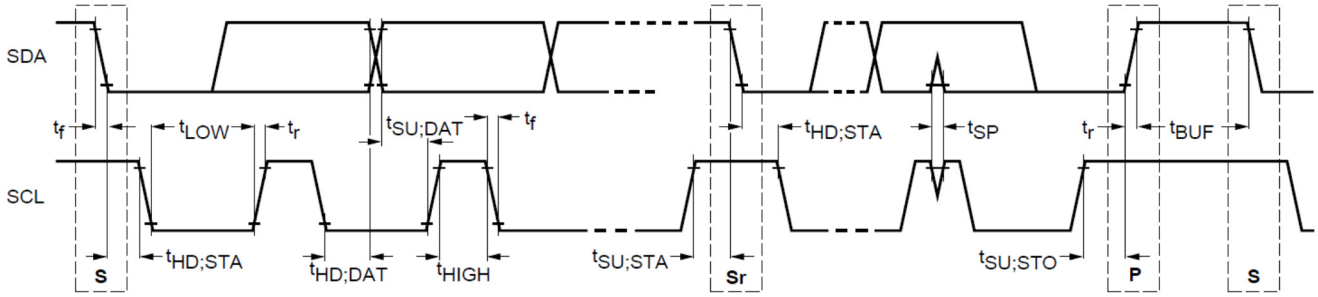
The actions that the host performs are up to the System Designer.

If multiple modules are faulting, SALRT will still be low after doing the above steps and will require transmission with the Alert Response Address repeatedly until all faults are cleared.

Please refer to the PMBus™ Commands section of this document for details on how to monitor specific parameters via the SMBus interface.

PMBUS™ SPECIFICATIONS

Timing Parameters For Higher Speed Operation



Parameter	Symbol	Standard-Mode Specs		Actual Measured		Unit
		Min	Max			
SCL clock frequency	f_{SCL}	10	400	100.05		KHz
Hold time (repeated) START condition	$t_{HD;STA}$	0.6	-	3.35		uS
LOW period of SCL clock	t_{LOW}	1.3	-	6.60		uS
HIGH period of SCL clock	t_{HIGH}	0.6	-	5.89		uS
Setup time for repeated START condition	$t_{SU;STA}$	0.6	-	5.83		uS
Data hold time	$t_{HD;DAT}$	300	-	3258		nS
Data setup time	$t_{SU;DAT}$	100	-	2406		nS
Rise time[1]	t_r	-	300	SCL = 222.0	SDA = 130.8	nS
Fall time[1]	t_f	-	300	SCL = 18.0	SDA = 12.0	nS
Setup time for STOP condition	$t_{SU;STO}$	0.6	-	5.86		uS
Bus free time between a STOP and START condition	t_{BUF}	1.3	-	2434.5		uS

Note 1: Rise and fall time is defined as follows:

$t_r = (V_{ILMAX} - 0.15)$ to $(V_{IHMIN} + 0.15)$

$t_f = 0.9\ V_{DD}$ to $(V_{ILMAX} - 0.15)$

PMBUS™ SPECIFICATIONS

LGA110D Support PMBus™ Command List

Command Code	Command Name	Default Value	Access Type	Data Bytes	Data Format	Description
01h	OPERATION	00h	R/W	1	BIT	Enable/disable, margin settings
02h	ON_OFF_CONFIG	17h	R/W	1	BIT	On/off configuration settings ENABLE pin control, active high
03h	CLEAR_FAULTS	N/A	Write	N/A	N/A	Clears faults
15h	STORE_USER_ALL	N/A	Write	N/A	N/A	Stores values to user store
16h	RESTORE_USER_ALL	N/A	Write	N/A	N/A	Restores values from user store
21h	VOUT_COMMAND	N/A	R/W	N/A	L16u	VSET/SA pin-strap setting. Sets nominal VOUT set-point
22h	VOUT_TRIM	0000h	R/W	2	L16s	Applies a trim voltage to VOUT set-point, default value is 0 V
23h	VOUT_CAL_OFFSET	0000h	R/W	2	L16s	Applies offset voltage to VOUT set-point, default value is 0 V
24h	VOUT_MAX	N/A	R/W	N/A	L16u	Sets maximum VOUT set-point, default value is 1.15*VOUT pin-strap setting
25h	VOUT_MARGIN_HIGH	N/A	R/W	N/A	L16u	Sets VOUT set-point during margin high, default value is 1.05*VOUT pin-strap setting
26h	VOUT_MARGIN_LOW	N/A	R/W	N/A	L16u	Sets VOUT set-point during margin low, default value is 0.95*VOUT pin strap setting
33h	FREQUENCY_SWITCH	N/A	R/W	N/A	L11	Sets switching frequency, default value is 500 KHz
37h	INTERLEAVE	0000h/ 0008h	R/W	N/A	BIT	Configures phase offset during group operation
40h	VOUT_OV_FAULT_LIMIT	N/A	R/W	N/A	L16u	Sets the VOUT overvoltage fault threshold, default value is 1.15*VOUT pin-strap setting
41h	VOUT_OV_FAULT_RESPONSE	N/A	R/W	1	BIT	Sets the VOUT overvoltage fault response, default value is disable, no retry
42h	VOUT_OV_WARN_LIMIT	N/A	R/W	2	L16u	Sets the VOUT overvoltage warning threshold, default value is 1.13*VOUT pin-strap setting
43h	VOUT_UV_WARN_LIMIT	N/A	R/W	2	L16u	Sets the VOUT overvoltage warning threshold, default value is 0.84*VOUT pin-strap setting
44h	VOUT_UV_FAULT_LIMIT	N/A	R/W	2	L16u	Sets the VOUT under voltage fault threshold, default value is 0.8*VOUT pin-strap setting
45h	VOUT_UV_FAULT_RESPONSE	N/A	R/W	1	BIT	Sets the VOUT under voltage fault response, default value is disable, no retry
4Fh	OT_FAULT_LIMIT	EBE8h	R/W	2	L11	Sets the over-temperature fault limit, default value is +125°C
50h	OT_FAULT_RESPONSE	N/A	R/W	1	BIT	Sets the over-temperature fault response, default value is disable, no retry
51h	OT_WARN_LIMIT	EB70h	R/W	2	L11	Sets the over-temperature warning limit, default value is +110°C
55h	VIN_OV_FAULT_LIMIT	D3E0h	R/W	2	L11	Sets the VIN overvoltage fault threshold, default value is 15.5 V
56h	VIN_OV_FAULT_RESPONSE	N/A	R/W	1	BIT	Sets the VIN overvoltage fault response, default value is disable, no retry
57h	VIN_OV_WARN_LIMIT	D3A0h	R/W	2	L11	Sets the VIN overvoltage warning threshold, default value is 14.5 V

PMBUS™ SPECIFICATIONS

LGA110D Support PMBus™ Command List

Command Code	Command Name	Default Value	Access Type	Data Bytes	Data Format	Description
58h	VIN_UV_WARN_LIMIT	CB99	R/W	2	L11	Sets the VIN under voltage warning Threshold, default value is 7.195 V
59h	VIN_UV_FAULT_LIMIT	CB73	R/W	2	L11	Sets the VIN under voltage fault threshold. UVLO pin-strap setting, default value is 6.898 V
5Ah	VIN_UV_FAULT_RESPONSE	N/A	R/W	1	BIT	Sets the VIN under voltage fault response, default value is disable, no retry
5Eh	POWER_GOOD_ON	N/A	R/W	2	L16u	Sets the voltage threshold for power-good indication, default value is 0.9*VSET pin-strap setting
60h	TON_DELAY	8000h	R/W	2	L11	Sets the delay time from enable to VOUT rise, default value is 0 ms
61h	TON_RISE	C300h	R/W	2	L11	Sets the rise time of VOUT after ENABLE and TON_DELAY, default value is 3 ms
64h	TOFF_DELAY	0000h	R/W	2	L11	Sets the delay time from DISABLE to start of VOUT fall, default value is 0 ms
65h	TOFF_FALL	CA80h	R/W	2	L11	Sets the fall time for VOUT after DISABLE and TOFF_DELAY, default value is 5 ms
78h	STATUS_BYTE	00h	R	1	BIT	First byte of STATUS_WORD, default value is no faults
79h	STATUS_WORD	0000h	R	2	BIT	Summary of critical faults, default value is no faults
7Ah	STATUS_VOUT	00h	R	1	BIT	Reports VOUT warnings/faults, default value is no faults
7Bh	STATUS_IOUT	00h	R	1	BIT	Reports IOUT warnings/faults, default value is no faults
7Ch	STATUS_INPUT	00h	R	1	BIT	Reports input warnings/faults, default value is no faults
7Dh	STATUS_TEMP	00h	R	1	BIT	Reports temperature warnings/faults, default value is no faults
7Eh	STATUS_CML	00h	R	1	BIT	Reports communication, memory, logic Errors, default value is no errors
80h	STATUS_MFR_SPECIFIC	00h	R	1	BIT	Reports voltage monitoring/clock synchronization faults, default value is no faults
88h	READ_VIN	N/A	R	2	L11	Reports input voltage measurement
8Bh	READ_VOUT	N/A	R	2	L16u	Reports output voltage measurement
8Ch	READ_IOUT	N/A	R	2	L11	Reports output current measurement
8Dh	READ_TEMPERATURE_1	N/A	R	2	L11	Reports internal temperature measurement
8Fh	READ_TEMPERATURE_3	N/A	R	2	L11	Reports external temperature measurement from Mosfet pin
94h	READ_DUTY_CYCLE	N/A	R	2	L11	Reports actual duty cycle
95h	READ_FREQUENCY	N/A	R	2	L11	Reports actual switching frequency
98h	PMBus_REVISION	33h	R	1	BIT	Reports the PMBus™ revision used, Part 1 Rev 1.3, Part 2 Rev 1.3
99h	MFR_ID	N/A	BR/BW	N/A	ASC	LGA110D-01DADJJ
9Bh	MFR_REVISION	303031	BR/BW	N/A	ASC	001
9Eh	MFR_SERIAL	N/A	R/W	N/A	ASC	Serial number
B0h	USER_DATA_00	Vo1=0x41 Vo2=0x42	R/W	N/A	ASC	Factory setting, define V_O1=A, V_O2=B

PMBUS™ SPECIFICATIONS

LGA110D Support PMBus™ Command List

Command Code	Command Name	Default Value	Access Type	Data Bytes	Data Format	Description
D1h	USER_CONFIG	Vo1=0x1016 Vo2=0x1015	R/W	2	BIT	Configures several user-level features, default value is V_O1=0x1016, V_O2=0x1015
D3h	DDC_CONFIG	N/A	R/W	2	BIT	Configures the DDC addressing and current sharing, default value is V_O1=0x0100, V_O2=0x0200
D4h	POWER_GOOD_DELAY	BA00h	R/W	2	L11	Sets the delay between PG threshold and PG assertion, default value is 1 ms
D5h	ASCR_ADVANCED	2320h	R/W	2	BIT	Sets ASCR Threshold and Threshold Gain, default value is Gain Select divide by 4, threshold 800
D7h	SNAPSHOT_FAULT_MASK	0000h	R/W	2	BIT	Masks faults that cause a snapshot to be taken, default value is no faults masked
DBh	MFR_SMBALERT_MASK	00…00h	R/W	7	BIT	Identifies which fault limits will not assert SALRT
DFh	ASCR_CONFIG	N/A	R/W	4	BIT	Configures the ASCR settings ASCR gain is ASCRCFG pin-strap setting, default integral gain is 50, default ASCR residual is 90
E0h	SEQUENCE	00h	R/W	1	BIT	DDC rail sequencing configuration, default value is prequel and sequel disabled
E2h	DDC_GROUP	00000000	R/W	4	BIT	Configures group ID, fault spreading, OPERATION and VOUT, default value is ignore broadcast, sequenced shutdown, and fault spreading
E3h	STORE_CONTROL	N/A	R/W	1	BIT	Stores command settings in the User and Default Stores while the device is enabled. Used in conjunction with STORE_DATA.
E5h	MFR_IOUT_OC_FAULT_RESPONSE	N/A	R/W	1	BIT	Configures the IOUT over current fault response, default value is disable, no retry
E6h	MFR_IOUT_UC_FAULT_RESPONSE	N/A	R/W	1	BIT	Configures the IOUT undercurrent fault response, default value is disable, no retry
E7h	IOUT_AVG_OC_FAULT_LIMIT	N/A	R/W	2	L11	Sets the IOUT average over current fault threshold for each phase, default value is 0.8 x IOUT_OC_FAULT_LIMIT pin-strap setting
E9h	ADVANCED_CONFIG	01h	R/W	1	BIT	Sets PWM mid-drive voltage, SMBus I/O and enable/disable the VG LDO
EAh	SNAPSHOT	N/A	Read	32	BIT	32-byte read-back of parametric and status values
F0h	LEGACY_FAULT_GROUP	00…00h	R/W	4	BIT	Configures fault group compatibility with older Artesyn digital power devices, default value is no fault groups selected
F2h	STORE_DATA	N/A	R/W	N/A	Custom	Stores command settings in the User and Default Stores while the device is enabled. Used in conjunction with STORE_CONTROL
F3h	SNAPSHOT_CONTROL	0800h	R/W	2	BIT	Snapshot feature control command
F4h	RESTORE_FACTORY	N/A	Write	N/A	N/A	Restores device to the hard-coded default values
F5h	PINSTRAP_READ_STATUS	N/A	Read	5	BIT	Reads back an index for each pin-strap setting, CFG, ASCRCFG, VSET/SA, SYNC, default value is pin-strap resistor indexes

PMBUS™ SPECIFICATIONS

LGA110D Support PMBus™ Command List

Command Code	Command Name	Default Value	Access Type	Data Bytes	Data Format	Description
F6h	IIN_CAL_OFFSET	8BD7h	R/W	2	L11	Sets an offset to IIN sense circuit, default value is 0.03 A
FAh	SECURITY_CONTROL	00h	R/W	1	BIT	Sets the security functions mode
FBh	PASSWORD	00…00h	Write	9	ASCII	Sets the private password string
FDh	WRITE_PROTECT	00…00h	R/W	32	Custom	Identifies which commands are protected

PMBUS™ SPECIFICATIONS

PMBus™ User Guidelines

The PMBus™ is a powerful tool that allows the user to optimize circuit performance by configuring the LGA110D for their application. When configuring the LGA110D, the LGA110D should be disabled whenever most settings are changed with PMBus commands. Some exceptions to this recommendation are OPERATION, ON_OFF_CONFIG, CLEAR_FAULTS, VOUT_COMMAND, VOUT_MARGIN_HIGH, VOUT_MARGIN_LOW. While the LGA110D is enabled any command can be read. Many commands do not take effect until after the LGA110D has been re-enabled, hence the recommendation that commands that change device settings are written while the LGA110D is disabled. When sending the STORE_DEFAULT_ALL, STORE_USER_ALL, RESTORE_DEFAULT_ALL and RESTORE_USER_ALL commands, it is recommended that no other commands are sent to the device for 100ms after sending STORE or RESTORE commands. In addition, there should be a 2 ms delay between repeated READ commands sent to the same device. When sending any other command, a 5 ms delay is recommended between repeated commands sent to the same device.

SUMMARY

All commands can be read at any time.

Always disable the LGA110D when writing commands that change device settings. Exceptions to this rule are commands intended to be written while the LGA110D is enabled, for example, VOUT_MARGIN_HIGH.

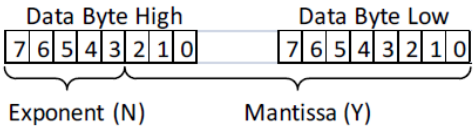
To be sure a change to LGA110D setting has taken effect, write the STORE_USER_ALL command, then cycle input power and re-enable the LGA110D.

PMBUS™ SPECIFICATIONS

PMBus™ Data Formats

Linear-11 (L11)

L11 data format uses 5-bit two's compliment exponent (N) and 11-bit two's compliment mantissa (Y) to represent real world decimal value (X).



Relation between real world decimal value (X), N and Y is: $X = Y \cdot 2^{N}$

Linear-16 Unsigned (L16u)

L16u data format uses a fixed exponent (hard-coded to N = -13h) and a 16-bit unsigned integer mantissa (Y) to represent real world decimal value (X). Relation between real world decimal value (X), N and Y is: $X = Y \cdot 2^{-13}$.

Linear-16 Signed (L16s)

L16s data format uses a fixed exponent (hard-coded to N = -13h) and a 16-bit two's compliment mantissa (Y) to represent real world decimal value (X). Relation between real world decimal value (X), N and Y is: $X = Y \cdot 2^{-13}$

Bit Field (BIT)

Breakdown of Bit Field is provided in "PMBus™ Command Detail".

Custom (CUS)

Breakdown of custom data format is provided in "PMBus™ Command Detail". A combination of bit field and integer is common type of custom data format.

ASCII (ASC)

A variable length string of text characters uses ASCII data format.

PMBUS™ SPECIFICATIONS

PMBus™ Command Detail

OPERATION (01h)

Definition: Sets Enable, Disable, and VOUT Margin settings. Writing immediate off to turns off the output and ignores TOFF_DELAY and TOFF_FALL settings. With Immediate off, the PWM signal is set to tri-state level without delay. This command is not stored like other PMBus commands. When this command is written, the command takes effect, but if a STORE _USER_ALL written and the device is re-enabled, the OPERATION settings may not be the same settings that were written before the device was re-enabled. This command reflects only the last value written. Read the STATUS_BYTE/WORD command for the enable state.

Data Length in Bytes: 1

Data Format: Bit Field

Type: R/W

Protectable: No

Default Value: 00h

Units: N/A

COMMAND	OPERATION (01h)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table							

BITS	PURPOSE	BIT VALUE	MEANING
7	Controls device output state	0	Off (see ON_OFF_CONFIG)
		1	On (see ON_OFF_CONFIG)
6	Turn off behavior. This bit is ignored if Bit 7 = 1.	0	Ignore TOFF_DELAY and TOFF_FALL
		1	Observe TOFF_DELAY and TOFF_FALL
5:4	Output voltage	00	VOUT is set by VOUT_COMMAND.
		01	VOUT is set by VOUT_MARGIN_LOW.
		10	VOUT is set by VOUT_MARGIN_HIGH.
		11	Not used
3:2	Margin fault response	00	Not used
		01	Faults caused by VOUT_MARGIN_HIGH or VOUT_MARGIN_LOW are ignored.
		10	Faults caused by VOUT_MARGIN_HIGH or VOUT_MARGIN_LOW are acted on.
		11	Not used
1:0	Not used	00	Not used

PMBUS™ SPECIFICATIONS

ON_OFF_CONFIG (02h)

Definition: Configures the interpretation and coordination of the OPERATION command and the Enable pin (EN). When Bit 0 is set to 1 (turn off the output immediately), the TOFF_FALL setting is ignored. Note: When Bit 3 and 2 are set to "1", the device turns on only when the EN pin is high and the OPERATION command instructs the device to enable. With Bit 3 and 2 set to "1", the device turns off when EN is set low or the OPERATION command instructs the device to disable.

Data Length in Bytes: 1

Data Format: Bit Field

Type: R/W

Protectable: Yes

Default Value: 17h (ENABLE pin control, active high, turn off output immediately – no ramp down)

Units: N/A

COMMAND	ON_OFF_CONFIG (02h)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table							
Default Value	0	0	0	1	0	1	1	1

BITS	PURPOSE	BIT VALUE	MEANING
7:5	Not used	000	Not used
4	Sets the default for the on/off behavior of the device to be controlled by the EN pin and OPERATION command	0	Device is always on.
		1	Device does not power up until commanded by the EN pin and OPERATION command (as programmed in Bits [3:0]).
3	Controls how the device responds to commands received through the PMBus	0	Device ignores the on/off portion of the OPERATION command.
		1	To start, the device requires that the on/off portion of the OPERATION command is instructing the device to enable the output. Depending on Bit 2, the device may also require the EN pin to be asserted for the device to start and enable the output.
2	Controls how the device responds to the EN pin	0	Device ignores the EN pin (on/off controlled only by the OPERATION command).
		1	Device requires the EN pin to be asserted to start the unit. Depending on Bit 3, the OPERATION command may also be required to instruct the device to start before the output is energized.
1	Polarity of EN pin - active low not used	0	Not used
		1	Active high only
0	EN pin action when commanding the unit to turn off	0	Use the configured ramp-down settings ("soft-off").
		1	Turn off the output immediately.

PMBUS™ SPECIFICATIONS

CLEAR_FAULTS (03h)

Definition: Clears all fault bits in all registers and releases the SALRT pin (if asserted) simultaneously. If a fault condition still exists, the bit will reassert immediately. This command will not restart a device if it has shut down, it will only clear the faults.

Data Length in Bytes: 0 Byte

Data Format: N/A

Type: Write only

Protectable: No

Default Value: N/A

Units: N/A

STORE_USER_ALL (15h)

Definition: Stores all PMBus™ settings from the operating memory to the non-volatile USER store memory. To clear the user store, perform a RESTORE_FACTORY then STORE_USER_ALL. To add to the user store, perform a RESTORE_USER_ALL, write commands to be added, then STORE_USER_ALL. This command should not be used during device operation, the device will be unresponsive for 100 ms while storing values.

Data Length in Bytes: 0

Data Format: N/A

Type: Write only

Protectable: Yes

Default Value: N/A

Units: N/A

RESTORE_USER_ALL (16h)

Definition: Restores PMBus settings from the non-volatile default store memory into the operating memory. These settings are loaded during at power-up if not superseded by settings in user store. Do not use this command during device operation; the device is unresponsive for 100 ms while storing values.

Data Length in Bytes: 0

Data Format: N/A

Type: Write only

Protectable: No

Default Value: N/A

Units: N/A

PMBUS™ SPECIFICATIONS

VOUT_COMMAND (21h)

Definition: Sets or reports the target output voltage. The integer value is multiplied by 2 raised to the power of -13h. This command cannot be set higher than VOUT_MAX. If a value is written to this command below or above the range given below, the device sets the value to the lower or upper limit, respectively, and a warning is recorded in STATUS_VOUT.

Data Length in Bytes: 2

Data Format: Linear-16 Unsigned

Type: R/W

Protectable: Yes

Default Value: VSET pin-strap setting

Units: V

Equation: VOUT = VOUT_COMMAND x 2^{-13}

Range: 0.1V to VOUT_MAX

Example: VOUT_COMMAND = 699Ah = 27034

Target voltage equals 27034 x 2^{-13} = 3.3 V

COMMAND	VOUT_COMMAND (21h)															
Format	Linear-16 Unsigned															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default Value	VSET/SA Pin-strap Setting															

VOUT_TRIM (22h)

Definition: Applies a fixed trim voltage to the output voltage command value. This command is typically used by the manufacturer of a power supply subassembly to calibrate a device in the subassembly circuit. The two bytes are formatted as a two's complement binary mantissa, used in conjunction with the exponent of -13h. Values outside of the range are not accepted.

Data Length in Bytes: 2

Data Format: Linear-16 Signed

Type: R/W

Protectable: Yes

Default Value: 0000h (0V)

Units: V

Equation: VOUT trim = VOUT_TRIM x 2^{-13}

Range: ±0.15 V

COMMAND	VOUT_TRIM (22h)															
Format	Linear-16 Unsigned															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

PMBUS™ SPECIFICATIONS

VOUT_CAL_OFFSET (23h)

Definition: Applies a fixed offset voltage to the output voltage command value. This command typically calibrates a device in the application circuit. The two bytes are formatted as a two's complement binary mantissa and used in conjunction with the exponent of -13h. Values outside of the range are not accepted.

Data Length in Bytes: 2

Data Format: Linear-16 Signed

Type: R/W

Protectable: Yes

Default Value: 0000h (0V)

Units: V

Equation: VOUT calibration offset = VOUT_CAL_OFFSET x 2^{-13}

Range: ±0.15 V

COMMAND	ON_OFF_CONFIG (23h)															
Format	Linear-16 Signed															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

VOUT_MAX (24h)

Definition: Sets an upper limit on the output voltage the unit can command regardless of any other commands or combinations. The intent of this command is to provide a safeguard against you accidentally setting the output voltage to a possibly destructive level rather than to be the primary output overprotection. A VOUT_COMMAND greater than the existing VOUT_MAX is not set and VOUT_COMMAND remains the same. If a VOUT_MAX sent is less than the current VOUT_COMMAND, output voltage is limited to VOUT_MAX. Values outside of the range are not accepted.

Data Length in Bytes: 2

Data Format: Linear-16 Unsigned

Type: R/W

Protectable: Yes

Default Value: 1.15 x VSET/SA pin-strap setting

Units: V

Equation: VOUT max = VOUT_MAX x 2^{-13}

Range: 0.1 V to 5.5 V

COMMAND	VOUT_MAX (24h)															
Format	Linear-16 Unsigned															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default Value	1.15 x VSET Pin-strap Setting															

PMBUS™ SPECIFICATIONS

VOUT_MARGIN_HIGH (25h)

Definition: Sets the value of the VOUT during a margin high. This VOUT_MARGIN_HIGH command loads the unit with the voltage to which the output is to be changed when the OPERATION command is set to “Margin High”. Values outside of the range are not accepted.

Data Length in Bytes: 2

Data Format: Linear-16 Signed

Type: R/W

Protectable: Yes

Default Value: 1.05 x VSET pin-strap setting.

Units: V

Equation: VOUT calibration offset = VOUT_CAL_OFFSET x 2^{-13}

Range: 0.1 V to VOUT_MAX

COMMAND	VOUT_MARGIN_HIGH (25h)															
Format	Linear-16 Unsigned															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default Value	1.05 x VSET Pin-strap Setting															

VOUT_MARGIN_LOW (26h)

Definition: Sets the value of the VOUT during a margin low. This VOUT_MARGIN_LOW command loads the unit with the voltage to which the output is to be changed when the OPERATION command is set to “Margin Low”. Values outside of the range are not accepted.

Data Length in Bytes: 2

Data Format: Linear-16 Unsigned

Type: R/W

Protectable: Yes

Default Value: 0.95 x VSET pin-strap setting

Units: V

Equation: VOUT margin low = VOUT_MARGIN_LOW

Range: 0.1 V to VOUT_MAX

COMMAND	VOUT_MARGIN_LOW (26h)															
Format	Linear-16 Unsigned															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default Value	0.95 x VSET Pin-strap Setting															

PMBUS™ SPECIFICATIONS

FREQUENCY_SWITCH (33h)

Definition: Sets the switching frequency of the device. The initial default value is defined by a pin-strap and this value can be overridden by writing this command. If an external SYNC is used, this value should be set as close as possible to the external clock value. The output must be disabled when writing this command. Available frequencies are defined by the equation f_{SW} = 30MHz/n, where 30 ≤ n ≤ 150. The actual switching frequency is the nearest available frequency to the FREQUENCY_SWITCH value.

Data Length in Bytes: 2

Data Format: Linear-11

Type: R/W

Protectable: Yes

Default Value: SYNC pin-strap setting

Units: KHz

Equation: FREQUENCY_SWITCH = Y x 2^N

Range: 450 KHz to 800 KHz

COMMAND	FREQUENCY_SWITCH (33h)															
Format	Linear-11															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	SYNC Pin-strapped Value															

PMBUS™ SPECIFICATIONS

INTERLEAVE (37h)

Definition: Configures the phase offset of a device that is sharing a common SYNC clock with other devices. A desired phase position is specified. INTERLEAVE sets the phase offset between individual devices, current sharing groups, and/or combinations of devices and current sharing groups. The phase offset is set automatically by default for devices within a single current sharing group.

Phase offset (in degrees) = [Rounded (Position*16/Number)]*22.5

Phase offsets greater than 360 degrees are “wrapped around” by subtracting 360 degrees.

Data Length in Bytes: 2

Data Format: Bit Field

Type: R/W

Protectable: Yes

Default Value: V_O1 = 0008h, V_O2 = 0000h

Units: N/A

COMMAND	INTERLEAVE (37h)															
Format	Bit Field															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table															
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BITS	PURPOSE	VALUE	DESCRIPTION
15:4	Reserved	0	Reserved
3:0	Order	0 to 15d	Device phase order in group

PMBUS™ SPECIFICATIONS

VOUT_OV_FAULT_LIMIT (40h)

Definition: Sets the VOUT overvoltage fault threshold. VOUT_OV_WARN_LIMIT must be set below the VOUT_OV_FAULT_LIMIT for fault responses with restart attempts to function properly. When the VOUT_OV_FAULT_RESPONSE is set to retry, a retry is not attempted until the output voltage falls below the VOUT_OV_WARN_LIMIT. In response to the VOUT_OV_FAULT_LIMIT being exceeded, the device sets the VOUT bit in STATUS_WORD, sets the VOUT_OV_FAULT bit in STATUS_VOUT, and notifies the host.

Data Length in Bytes: 2

Data Format: Linear-16 Unsigned

Type: R/W

Protectable: Yes

Default Value: 1.15 x VSET pin-strap setting.

Units: V

Equation: VOUT OV fault limit = VOUT_OV_FAULT_LIMIT x 2^{-13}

Range: 0 V to 6.0 V

COMMAND	VOUT_OV_FAULT_LIMIT (40h)															
Format	Linear-16 Unsigned															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default Value	1.15 x VSET/SA Pin-strap Setting															

VOUT_OV_FAULT_RESPONSE (41h)

Definition: Configures the VOUT overvoltage fault response between latch off or retry continuously. The delay time is the time between fault detected to restart attempts. It's highly recommended set as default "no retires" Artesyn qualified only.

Data Length in Bytes: 1

Data Format: Bit Field

Type: R/W

Protectable: Yes

Default Value: CFG pin-strap setting

Units: Retry time = 35 ms increments

COMMAND	VOUT_OV_FAULT_RESPONSE (41h)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table							
Default Value	CFG Pin-strap Setting							

PMBUS™ SPECIFICATIONS

BITS	FIELD NAME	VALUE	DESCRIPTION
7:6	Response behavior, the device: • Pulls SALRT low • Sets the related fault bit in the status registers. Fault bits are only cleared by the CLEAR_FAULTS command.	00-01,11	Not used
		10	Disable and retry according to the setting in Bits [5:3].
5:3	Retry Setting	000	No retry. The output remains disabled until the device is restarted.
		001-111	Attempts to restart continuously until it is commanded OFF (by the EN pin, the OPERATION command, or both), bias power is removed, or another fault condition causes the unit to shut down. A retry is attempted after the output voltage falls below the VOUT_OV_WARN_LIMIT. The time between the start of each attempt to restart is set by the value in Bits [2:0].
2:0	Retry Delay	000-111	Retry delay time = (Value + 1)*35 ms. Sets the time between retries in 35 ms increments. Range is 35 ms to 280 ms.

VOUT_OV_WARN_LIMIT (42h)

Definition: Sets the VOUT overvoltage warning threshold. VOUT_OV_WARN_LIMIT must be set below the VOUT_OV_FAULT_LIMIT for fault responses with restart attempts to function properly. When the VOUT_OV_FAULT_RESPONSE is set to retry, a retry is not attempted until the output voltage falls below the VOUT_OV_WARN_LIMIT. In response to the VOUT_OV_WARN_LIMIT being exceeded, the device sets the VOUT bit in STATUS_WORD, sets the VOUT_OV_WARNING bit in STATUS_VOUT, and notifies the host. In the case of a fast VOUT overvoltage transition, a VOUT_OV_WARN_LIMIT fault may not be recorded.

Data Length in Bytes: 2

Data Format: Linear-16 Unsigned

Type: R/W

Protectable: Yes

Default Value: 1.13 x VSET pin-strap setting.

Units: V

Equation: VOUT OV fault limit = VOUT_OV_FAULT_LIMIT x 2^{-13}

Range: 0 V to 5.5 V

COMMAND	VOUT_OV_WARN_LIMIT (42h)															
Format	Linear-16 Unsigned															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default Value	1.13 x VSET Pin-strap Setting															

PMBUS™ SPECIFICATIONS

VOUT_UV_WARN_LIMIT (43h)

Definition: Sets the VOUT undervoltage warn threshold. This fault is masked during ramp, before Power-Good is asserted or when the device is disabled. VOUT_UV_WARN_LIMIT must be set to a value below POWER_GOOD_ON and above VOUT_UV_FAULT_LIMIT. In response to the VOUT_UV_WARN_LIMIT being exceeded, the devices sets the VOUT bit in STATUS_WORD, sets the VOUT_UV_WARNING bit in STATUS_VOUT, and notifies the host.

Data Length in Bytes: 2

Data Format: Linear-16 Unsigned

Type: R/W

Protectable: Yes

Default Value: 0.84 x VSET pin-strap setting.

Units: V

Equation: VOUT UV fault limit = VOUT_UV_FAULT_LIMIT x 2^{-13}

Range: 0 V to 5.5 V

COMMAND	VOUT_UV_WARN_LIMIT (43h)															
Format	Linear-16 Unsigned															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default Value	0.84 x VSET Pin-strap Setting															

VOUT_UV_FAULT_LIMIT (44h)

Definition: Sets the VOUT undervoltage fault threshold. This fault is masked during ramp, before power-good is asserted or when the device is disabled. VOUT_UV_FAULT_LIMIT must be set to a value below VOUT_UV_WARN_LIMIT and POWER_GOOD_ON. In response to the VOUT_UV_FAULT_LIMIT being exceeded, the device: Sets the VOUT bit in STATUS_WORD, sets the VOUT_UV_FAULT bit in STATUS_VOUT and notifies the host.

Data Length in Bytes: 2

Data Format: Linear-16 Unsigned

Type: R/W

Protectable: Yes

Default Value: 0.8 x VSET pin-strap setting.

Units: V

Equation: VOUT UV fault limit = VOUT_UV_FAULT_LIMIT x 2^{-13}

Range: 0 V to 5.5 V

COMMAND	VOUT_UV_FAULT_LIMIT (44h)															
Format	Linear-16 Unsigned															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default Value	0.8 x VSET Pin-strap Setting															

PMBUS™ SPECIFICATIONS

VOUT_UV_FAULT_RESPONSE (45h)

Definition: Configures the VOUT undervoltage fault response. Note: VOUT UV faults can only occur after Power-good (PG) has been asserted. Under some circumstances this causes the output to stay fixed below the power-good threshold indefinitely. If this behavior is undesired, use setting 80h. The delay time is the time between fault detected to restart attempts. TON_DELAY is still observed during a retry attempt after the retry delay has expired.

Data Length in Bytes: 1

Data Format: Bit Field

Type: R/W

Protectable: Yes

Default Value: CFG pin-strap setting

Units: Retry time unit = 35 ms

COMMAND	VOUT_UV_FAULT_RESPONSE (45h)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table							
Default Value	CFG Pin-strap Setting							

BITS	FIELD NAME	VALUE	DESCRIPTION
7:6	Response behavior, the device: • Pulls SALRT low • Sets the related fault bit in the status registers. Fault bits are only cleared by the CLEAR_FAULTS command.	00-01,11	Not used
		10	Disable and retry according to the setting in Bits [5:3]
5:3	Retry Setting	000	No retry. The output remains disabled until the fault is cleared.
		001-111	Attempts to restart continuously, until it is commanded OFF (by the EN pin or OPERATION command or both), bias power is removed, or another fault condition causes the unit to shut down. The time between the start of each attempt to restart is set by the value in Bits [2:0].
2:0	Retry Delay	000-111	Retry delay time = (Value +1)*35 ms. Sets the time between retries in 35 ms increments. Range is 35 ms to 280 ms.

PMBUS™ SPECIFICATIONS

OT_FAULT_LIMIT (4Fh)

Definition: Sets the temperature at which the device should indicate an over-temperature fault. OT_WARN_LIMIT must be set below the OT_FAULT_LIMIT for fault responses with restart attempts to function properly. When the OT_FAULT_RESPONSE is set to retry, a retry is not attempted until the temperature falls below the OT_WARN_LIMIT. In response to the OT_FAULT_LIMIT being exceeded, the device sets the TEMPERATURE bit in STATUS_WORD, sets the OT_FAULT bit in STATUS_TEMPERATURE, and notifies the host. Note: Voltages above 2.5V on the TMON pin cause the device to automatically shut down and latch off, regardless of the OT_FAULT_LIMIT setting or if TMON is being used for over-temperature faults. This fault is recorded in Bit 1 of STATUS_MFR_SPECIFIC.

Data Length in Bytes: 2

Data Format: Linear-11

Type: R/W

Protectable: Yes

Default Value: EBE8h (+125^{O}C)

Units: ^{O}C

Equation: OT_FAULT_LIMIT = Y x 2^{N}

Range: 0 to 175^{O}C

COMMAND	OT_FAULT_LIMIT (4Fh)															
Format	Linear-11															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	1	1	1	0	1	0	1	1	1	1	1	0	1	0	0	0

OT_FAULT_RESPONSE (50h)

Definition: Instructs the device on what action to take in response to an over-temperature fault. The delay time is the time between fault detected and restart attempts.

Data Length in Bytes: 1

Data Format: Bit Field

Type: R/W

Protectable: Yes

Default Value: CFG Pin-strap setting

Units: Retry time unit = 35 ms

COMMAND	OT_FAULT_RESPONSE (50h)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table							
Default Value	CFG Pin-strap Setting							

PMBUS™ SPECIFICATIONS

BITS	FIELD NAME	VALUE	DESCRIPTION
7:6	Response behavior, the device: • Pulls SALRT low • Sets the related fault bit in the status registers. Fault bits are only cleared by the CLEAR_FAULTS command.	00-01,11	Not used
		10	Disable and retry according to the setting in Bits [5:3]
5:3	Retry Setting	000	No retry. The output remains disabled until the fault is cleared.
		001-111	Attempts to restart continuously, until it is commanded OFF (by the EN pin, OPERATION command, or both), bias power is removed, or another fault condition causes the unit to shut down. A retry is attempted after the temperature falls below the OT_WARN_LIMIT. The time between the start of each attempt to restart is set by the value in Bits [2:0].
2:0	Retry Delay	000-111	Retry delay time = (Value +1)*35 ms. Sets the time between retries in 35 ms increments. Range is 35 ms to 280 ms.

OT_WARN_LIMIT (51h)

Definition: Sets the temperature at which the device should indicate an over-temperature warning alarm. OT_WARN_LIMIT must be set below the OT_FAULT_LIMIT for fault responses with restart attempts to function properly. When the OT_FAULT_RESPONSE is set to retry, a retry is not attempted until the temperature falls below the OT_WARN_LIMIT. In response to the OT_WARN_LIMIT being exceeded, the device sets the TEMPERATURE bit in STATUS_WORD, sets the OT_WARNING bit in STATUS_TEMPERATURE, and notifies the host.

Data Length in Bytes: 2

Data Format: Linear-11

Type: R/W

Protectable: Yes

Default Value: EB70h (+110^{O}C)

Units: ^{O}C

Equation: OT_WARN_LIMIT = Y x 2^{N}

Range: 0 to 175^{O}C

COMMAND	OT_WARN_LIMIT (51h)															
Format	Linear-11															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	1	1	1	0	1	0	1	1	0	1	1	1	0	0	0	0

PMBUS™ SPECIFICATIONS

VIN_OV_FAULT_LIMIT (55h)

Definition: Sets the VIN overvoltage fault threshold. VIN_OV_WARN_LIMIT must be set below the VIN_OV_FAULT_LIMIT for fault responses with restart attempts to function properly. When the VIN_OV_FAULT_RESPONSE is set to retry, a retry is not attempted until the input voltage falls below the VIN_OV_WARN_LIMIT. Values outside of the range are not accepted.

Data Length in Bytes: 2

Data Format: Linear-11

Type: R/W

Protectable: Yes

Default Value: D3E0h (15.5 V)

Units: V

Equation: VIN_OV_FAULT_LIMIT = Y x 2^N

Range: 0V to 15.5 V

COMMAND	VIN_OV_FAULT_LIMIT (55h)															
Format	Linear-11															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Signed Exponent, N								Signed Mantissa, Y							
Default Value	1	1	0	1	0	0	1	1	1	1	1	0	0	0	0	0

VIN_OV_FAULT_RESPONSE (56h)

Definition: Configures the VIN overvoltage fault response as defined by the table below. It's highly recommended set as default "no retry" qualified only.

Data Length in Bytes: 1

Data Format: Bit Field

Type: R/W

Protectable: Yes

Default Value: CFG pin-strap setting

Units: N/A

COMMAND	VIN_OV_FAULT_RESPONSE (56h)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table							
Default Value	CFG Pin-strap Setting							

PMBUS™ SPECIFICATIONS

BITS	FIELD NAME	VALUE	DESCRIPTION
7:6	Response behavior, the device: • Pulls SALRT low • Sets the related fault bit in the status registers. Fault bits are only cleared by the CLEAR_FAULTS command.	00-01,11	Not used
		10	Disable and retry according to the setting in Bits [5:3]
5:3	Retry Setting	000	No retry. The output remains disabled until the fault is cleared.
		001-111	Attempts to restart continuously, until it is commanded OFF (by the EN pin, OPERATION command, or both), bias power is removed, or another fault condition causes the unit to shut down. A retry is attempted after the input voltage falls below the VIN_OV_WARN_LIMIT. The time between the start of each attempt to restart is set by the value in Bits [2:0].
2:0	Retry Delay	000-111	Retry delay time = (Value +1)*35 ms. Sets the time between retries in 35 ms increments. Range is 35 ms to 280 ms.

VIN_OV_WARN_LIMIT (57h)

Definition: Sets the VIN overvoltage warning threshold as defined by the table below. VIN_OV_WARN_LIMIT must be set below the VIN_OV_FAULT_LIMIT for fault responses with restart attempts to function properly. When the VIN_OV_FAULT_RESPONSE is set to retry, a retry is not attempted until the input voltage falls below the VIN_OV_WARN_LIMIT. In response to the OV_WARN_LIMIT being exceeded, the device sets the INPUT bits in STATUS_WORD, sets the VIN_OV_WARNING bit in STATUS_INPUT, and notifies the host. Values outside of the range are not accepted.

Data Length in Bytes: 2

Data Format: Linear-11

Type: R/W

Protectable: Yes

Default Value: D3A0h (14.5 V)

Units: V

Equation: VIN_OV_FAULT_LIMIT = Y x 2^N

Range: 0 V to 19 V

COMMAND	VIN_OV_WARN_LIMIT (57h)															
Format	Linear-11															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	1	1	0	1	0	0	1	1	1	0	1	0	0	0	0	0

PMBUS™ SPECIFICATIONS

VIN_UV_WARN_LIMIT (58h)

Definition: Sets the VIN undervoltage warning threshold. VIN_UV_WARN_LIMIT must be set above the VIN_UV_FAULT_LIMIT for fault responses with restart attempts to function properly. When the VIN_UV_FAULT_RESPONSE is set to retry, a retry is not attempted until the input voltage rises above the VIN_UV_WARN_LIMIT. In response to the input voltage falling below VIN_UV_WARN_LIMIT, the device sets the INPUT bits in STATUS_WORD, sets the VIN_UV_WARNING bit in STATUS_INPUT, and notifies the host. Values outside of the range are not accepted.

Data Length in Bytes: 2

Data Format: Linear-11

Type: R/W

Protectable: Yes

Default Value: CB99 (7.195 V)

Units: V

Equation: VIN_UV_WARN_LIMIT = Y x 2^N

Range: 0V to 16V

COMMAND	VIN_UV_WARN_LIMIT (58h)															
Format	Linear-11															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	1	1	0	0	1	0	1	1	1	0	0	1	1	0	0	1

VIN_UV_FAULT_LIMIT (59h)

Definition: Sets the VIN undervoltage fault threshold. VIN_UV_WARN_LIMIT must be set above the VIN_UV_FAULT_LIMIT for fault responses with restart attempts to function properly. When the VIN_UV_FAULT_RESPONSE is set to retry, a retry is not attempted until the input voltage rises above the VIN_UV_WARN_LIMIT. In response to the input voltage falling below VIN_UV_FAULT_LIMIT, the device sets the INPUT bits in STATUS_WORD, sets the VIN_UV_FAULT bit in STATUS_INPUT, and notifies the host. Values outside of the range are not accepted.

Data Length in Bytes: 2

Data Format: Linear-11

Type: R/W

Protectable: Yes

Default Value: CB73h (6.898 V)

Units: V

Equation: VIN_UV_WARN_LIMIT = Y x 2^N

Range: 0 V to 16 V

COMMAND	VIN_UV_FAULT_LIMIT (59h)															
Format	Linear-11															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	1	1	0	0	1	0	1	1	0	1	1	1	0	0	1	1

PMBUS™ SPECIFICATIONS

VIN_UV_FAULT_RESPONSE (5Ah)

Definition: Configures the VIN under voltage fault response as defined by the table below. The delay time is the time between restart attempts. It's highly recommended set as default "no retry" qualified only.

Data Length in Bytes: 1

Data Format: Bit Field

Type: R/W

Protectable: Yes

Default Value: CFG pin-strap setting

Units: Retry time unit = 35 ms

COMMAND	VIN_UV_FAULT_RESPONSE (5Ah)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table							
Default Value	CFG Pin-strap Setting							

BIT NUMBER	FIELD NAME	VALUE	DESCRIPTION
7:6	Response behavior, the device: • Pulls SALRT low • Sets the related fault bit in the status registers. Fault bits are only cleared by the CLEAR_FAULTS command.	00-01,11	Not used
		10	Disable and retry according to the setting in Bits [5:3]
5:3	Retry Setting	000	No retry. The output remains disabled until the fault is cleared.
		001-111	Attempts to restart continuously, until it is commanded OFF (by the EN pin, OPERATION command, or both), bias power is removed, or another fault condition causes the unit to shut down. A retry is attempted after the input voltage rises above the VIN_UV_WARN_LIMIT. The time between the start of each attempt to restart is set by the value in Bits [2:0].
2:0	Retry Delay	000-111	Retry delay time = (Value+1)*35 ms. Sets the time between retries in 35 ms increments. Range is 35 ms to 280 ms.

PMBUS™ SPECIFICATIONS

POWER_GOOD_ON (5Eh)

Definition: Sets the voltage threshold for power-good indication. Power-good asserts when the output voltage exceeds POWER_GOOD_ON and deasserts when the output voltage is less than VOUT_UV_WARN_LIMIT. POWER_GOOD_ON should be set to a value above VOUT_UV_WARN_LIMIT. Power-good may not assert if the device is enabled for less than 2ms.

Data Length in Bytes: 2

Data Format: Linear-16 Unsigned

Type: R/W

Protectable: Yes

Default Value: 0.9 x VSET pin-strap setting.

Units: V

Range: 0 V to 5.5 V

COMMAND	POWER_GOOD_ON (5Eh)															
Format	Linear-16 Unsigned															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default Value	0.9 x VSET Pin-strap Setting															

TON_DELAY (60h)

Definition: Sets the delay time from when the device is enabled to the start of VOUT rise. Values outside of the range are not accepted.

Data Length in Bytes: 2

Data Format: Linear-11

Type: R/W

Protectable: Yes

Default Value: 8000h (0 ms)

Units: milliseconds (ms)

Equation: TON_DELAY = Y x 2^N

Range: 0 ms to 125 ms

COMMAND	TON_DELAY (60h)															
Format	Linear-11															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

PMBUS™ SPECIFICATIONS

TON_RISE (61h)

Definition: Sets the rise time of VOUT after the TON_DELAY time has elapsed. Values outside of the range are not accepted.

Data Length in Bytes: 2

Data Format: Linear-11

Type: R/W

Protectable: Yes

Default Value: C300h (3 ms)

Units: milliseconds (ms)

Equation: TON_RISE = Y x 2^N

Range: 0 ms to 125 ms. Although values can be set below 0.50 ms, rise time accuracy cannot be guaranteed. In addition, short rise times may cause excessive input and output currents to flow, thus triggering overcurrent faults at startup.

COMMAND	TON_RISE (61h)															
Format	Linear-11															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	1	1	0	0	0	0	1	1	0	0	0	0	0	0	0	0

TOFF_DELAY (64h)

Definition: Sets the delay time from DISABLE to start of VOUT ramps down. Values outside of the range are not accepted.

Data Length in Bytes: 2

Data Format: Linear-11

Type: R/W

Protectable: Yes

Default Value: 8000h (0 ms)

Units: milliseconds (ms)

Equation: TON_DELAY = Y x 2^N

Range: 0 ms to 125 ms

COMMAND	TOFF_DELAY (64h)															
Format	Linear-11															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

PMBUS™ SPECIFICATIONS

TOFF_FALL (65h)

Definition: Sets the fall time for VOUT after the TOFF_DELAY has expired. Setting the TOFF_FALL to values less than 0.5ms causes the device to turn off both the high-side and low-side FETs immediately after the expiration of the TOFF_DELAY time. Values outside of the range are not accepted.

Data Length in Bytes: 2

Data Format: Linear-11

Type: R/W

Protectable: Yes

Default Value: CA80h (5 ms)

Units: milliseconds (ms)

Equation: TOFF_FALL = Y x 2^N

Range: 0 ms to 125 ms. Values less than 0.5ms cause the device to turn off both the high-side and low-side FETs immediately after the expiration of the TOFF_DELAY time.

COMMAND	TOFF_FALL (65h)															
Format	Linear-11															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	1	1	0	0	1	0	1	0	1	0	0	0	0	0	0	0

PMBUS™ SPECIFICATIONS

STATUS_BYTE (78h)

Definition: Returns two bytes of information with a summary of the unit's fault condition. Based on the information in these bytes, the host can get more information by reading the appropriate status registers. The low byte of the STATUS_WORD (79h) is the same register as the STATUS_BYTE command.

Data Length in Bytes: 1

Data Format: Bit Field

Type: Read only

Protectable: Yes (read only)

Default Value: 00h (no faults)

Units: N/A

COMMAND	STATUS_BYTE (78h)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function	See Following Table							
Default Value	0	0	0	0	0	0	0	0

BITS	STATUS BIT NAME	MEANING
7	BUSY	Not used
6	OFF	This bit is asserted if the unit is not providing power to the output, regardless of the reason, including simply not being enabled.
5	VOUT_OV_FAULT	An output overvoltage fault occurred.
4	IOUT_OC_FAULT	An output overcurrent fault occurred.
3	VIN_UV_FAULT	An input undervoltage fault occurred.
2	TEMPERATURE	A temperature fault or warning occurred.
1	CML	A communications, memory or logic fault occurred.
0	Not used	Not used

PMBUS™ SPECIFICATIONS

STATUS_WORD (79h)

Definition: Returns two bytes of information with a summary of the unit's fault condition. Based on the information in these bytes, the host can get more information by reading the appropriate status registers. The low byte of the STATUS_WORD is the same register as the STATUS_BYTE (78h) command.

Data Length in Bytes: 2

Data Format: Bit Field

Type: Read only

Protectable: Yes (read only)

Default Value: 0000h (no faults)

Units: N/A

COMMAND	STATUS_WORD (79h)															
Format	Linear-11															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	See Following Table															
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BITS	STATUS BIT NAME	MEANING
15	VOUT	An output voltage fault or warning occurred.
14	IOUT	An output current fault occurred.
13	INPUT	An input voltage fault or warning occurred.
12	MFG_SPECIFIC	A manufacturer specific fault or warning occurred.
11	POWER_GOOD#	The POWER_GOOD signal, if present, is negated.[1]
10	Not Used	Not Used
9	OTHER	A bit in STATUS_VOUT, STATUS_IOUT, STATUS_INPUT, STATUS_TEMPERATURE, STATUS_CML, or STATUS_MFR_SPECIFIC is set.
8	Not Used	Not Used
7	Not Used	Not Used
6	OFF	This bit is asserted if the unit is not providing power to the output, regardless of the reason, including simply not being enabled.
5	VOUT_OV_FAULT	An output overvoltage fault occurred.
4	VOUT_OC_FAULT	An output overcurrent fault occurred.
3	VIN_UV_FAULT	An input undervoltage fault occurred.
2	TEMPERATURE	A temperature fault or warning occurred.
1	CML	A communications, memory or logic fault occurred.
0	Not Used	Not Used

Note 1: If the POWER_GOOD# bit is set, this indicates that the POWER_GOOD signal, if present, is signaling that the output power is not good. POWER_GOOD may not assert if the device is enabled for less than 2ms.

PMBUS™ SPECIFICATIONS

STATUS_VOUT (7Ah)

Definition: Returns one data byte with the status of the output voltage. Note: Warning bits may not be set when the corresponding fault bits are set. This can occur with rapidly changing fault waveforms.

Data Length in Bytes: 1

Data Format: Bit Field

Type: Read only

Protectable: Yes (read only)

Default Value: 00h (no faults)

Units: N/A

COMMAND	STATUS_VOUT (7Ah)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function	See Following Table							
Default Value	0	0	0	0	0	0	0	0

BITS	STATUS BIT NAME	MEANING
7	VOUT_OV_FAULT	Indicates an output overvoltage fault.
6	VOUT_OV_WARNING	Indicates an output overvoltage warning. Cannot be set when an overvoltage fault occurs.
5	VOUT_UV_WARNING	Indicates an output undervoltage warning. Cannot be set when an undervoltage fault occurs.
4	VOUT_UV_FAULT	Indicates an output under voltage fault.
3	VOUT_MAX_WARNING	Attempted to set VOUT_COMMAND greater than VOUT_MAX or below 0.1 V.
2:0	Not Used	Not Used

PMBUS™ SPECIFICATIONS

STATUS_IOUT (7Bh)

Definition: Returns one data byte with the status of the output current. Note: Warning bits may not be set when the corresponding fault bits are set. This can occur with rapidly changing fault waveforms.

Data Length in Bytes: 1

Data Format: Bit Field

Type: Read only

Protectable: Yes (read only)

Default Value: 00h (no faults)

Units: N/A

COMMAND	STATUS_IOUT (7Bh)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function	See Following Table							
Default Value	0	0	0	0	0	0	0	0

BITS	STATUS BIT NAME	MEANING
7	IOUT_OC_FAULT	An output over current fault has occurred.
6	Not Used	Not Used
5	IOUT_OC_WARNING	An output overcurrent warning occurred. Cannot be set when an output overcurrent fault occurs.
4	IOUT_UC_FAULT	An output undercurrent fault has occurred.
3:0	Not Used	Not Used

PMBUS™ SPECIFICATIONS

STATUS_INPUT (7Ch)

Definition: Returns one byte of information with a summary of input voltage related faults or warnings. Note: Warning bits may not be set when the corresponding fault bits are set. This can occur with rapidly changing fault waveforms.

Data Length in Bytes: 1

Data Format: Bit Field

Type: Read only

Protectable: Yes (read only)

Default Value: 00h (no faults)

Units: N/A

COMMAND	STATUS_INPUT (7Ch)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function	See Following Table							
Default Value	0	0	0	0	0	0	0	0

BITS	STATUS BIT NAME	MEANING
7	VIN_OV_FAULT	An input overvoltage fault occurred.
6	VIN_OV_WARNING	An input overvoltage warning occurred. Cannot be set when an overvoltage fault occurs.
5	VIN_UV_WARNING	An input undervoltage warning occurred. Cannot be set when an undervoltage fault occurs.
4	VIN_UV_FAULT	An input undervoltage fault occurred.
3:0	Not Used	Not Used

PMBUS™ SPECIFICATIONS

STATUS_TEMPERATURE (7Dh)

Definition: Returns one byte of information with a summary of any temperature related faults or warnings. Note: Warning bits may not be set when the corresponding fault bits are set. This can occur with rapidly changing fault waveforms.

Data Length in Bytes: 1

Data Format: Bit Field

Type: Read only

Protectable: Yes (read only)

Default Value: 00h (no faults)

Units: N/A

COMMAND	STATUS_TEMP (7Dh)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function	See Following Table							
Default Value	0	0	0	0	0	0	0	0

BITS	STATUS BIT NAME	MEANING
7	OT_FAULT	An over-temperature fault occurred.
6	OT_WARNING	An over-temperature warning occurred. Cannot be set when an over-temperature fault occurs.
5	UT_WARNING	An under-temperature warning occurred. Cannot be set when an under-temperature fault occurs.
4	UV_FAULT	An under-temperature fault occurred.
3:0	Not Used	Not Used

PMBUS™ SPECIFICATIONS

STATUS_CML (7Eh)

Definition: Returns one byte of information with a summary of any communications, logic, and/or memory errors. Status bits can only be cleared with the CLEAR_FAULTS command or by disabling, then re-enabling the device.

Data Length in Bytes: 1

Data Format: Bit Field

Type: Read only

Protectable: Yes (read only)

Default Value: 00h (no faults)

Units: N/A

COMMAND	STATUS_CML (7Eh)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function	See Following Table							
Default Value	0	0	0	0	0	0	0	0

BITS	MEANING
7	Invalid or unsupported PMBus™ command was received.
6	The PMBus™ command was sent with invalid or unsupported data.
5	A Packet Error Check (PEC) failed on a PMBus™ command.
4:2	Not Used
1	A PMBus™ command tried to write to a read-only or protected command, or too few or too many bytes were received for a given command
0	Not Used

PMBUS™ SPECIFICATIONS

STATUS_MFR_SPECIFIC (80h)

Definition: Returns one byte of information providing the status of miscellaneous system faults.

Data Length in Bytes: 1

Data Format: Bit Field

Type: Read Only

Protectable: Yes (read only)

Default Value: 00h (no faults)

Units: N/A

COMMAND	STATUS_MFR_SPECIFIC (80h)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function	See Following Table							
Default Value	0	0	0	0	0	0	0	0

BIT NUMBER	FIELD NAME	MEANING
7	Not Used	Not Used
6	Phase Fault	A phase in the current sharing group has failed, when configured as part of a current sharing rail.
5	Not Used	Not Used
4	DDC fault	An error was detected on the DDC bus.
3	External Switching Period Fault	Loss of external clock synchronization has occurred.
2	Fault Group	A fault was spread using DDC fault group.
1	SPS Fault	The SPS device set the TMON voltage above 2.5 V to indicate a general SPS fault.
0	Fault Bus	Device was shutdown by the enable pin when using the enable pin as a fault bus.

PMBUS™ SPECIFICATIONS

READ_VIN (88h)

Definition: Returns the input voltage reading.

Data Length in Bytes: 2

Data Format: Linear-11

Type: Read only

Protectable: Yes (read only)

Default Value: N/A

Units: V

Equation: READ_VIN = Y x 2^N

Range: N/A

COMMAND	READ_VIN (88h)															
Format	Linear-11															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	N/A															

READ_VOUT (8Bh)

Definition: Returns the output voltage reading.

Data Length in Bytes: 2

Data Format: Linear-16 Unsigned

Type: Read Only

Protectable: Yes (read only)

Default Value: N/A

Units: V

Equation: READ_VOUT = READ_VOUT x 2^{-13}

Range: N/A

COMMAND	READ_VOUT (8Bh)															
Format	Linear-16 Unsigned															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Default Value	N/A															

PMBUS™ SPECIFICATIONS

READ_IOUT (8Ch)

Definition: Returns the output current reading. No reading is returned if the PWM output is not active; that is, the output is not being regulated. It is not accurate when the device is in Diode Emulation Mode (DEM).

Data Length in Bytes: 2

Data Format: Linear-11

Type: Read only

Protectable: Yes (read only)

Default Value: N/A

Units: A

Equation: READ_IOUT = Y x 2^N

Range: N/A

COMMAND	READ_IOUT(8Ch)															
Format	Linear-11															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	N/A															

READ_TEMPERATURE_1 (8Dh)

Definition: Returns the temperature reading internal to the device.

Data Length in Bytes: 2

Data Format: Linear-11

Type: Read only

Protectable: Yes (read only)

Default Value: N/A

Units: °C

Equation: READ_TEMPERATURE_1 = Y x 2^N

Range: N/A

COMMAND	READ_TEMPERATURE_1 (8Dh)															
Format	Linear-11															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	N/A															

PMBUS™ SPECIFICATIONS

READ_TEMPERATURE_3 (8Fh)

Definition: Returns the temperature reading from the TMON pin. The voltage is read on this pin and converted to a temperature by the following equation: T ^{O}C = (Vtmon - 0.6 V)/0.008. Note: Voltages above 2.5 V on the TMON pin cause the device to automatically shut down and latch off, regardless of the OT_FAULT_LIMIT setting when using TMON for over-temperature faults.

Data Length in Bytes: 2

Data Format: Linear-11

Type: Read only

Protectable: Yes (read only)

Default Value: N/A

Units: ^{O}C

Equation: READ_TEMPERATURE_3 = Y x 2^{N}

Range: N/A

COMMAND	READ_TEMPERATURE_3 (8Fh)															
Format	Linear-11															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	N/A															

READ_DUTY_CYCLE (94h)

Definition: Reports the actual duty cycle of the converter while the device is enabled.

Data Length in Bytes: 2

Data Format: Linear-11

Type: Read only

Protectable: Yes (read only)

Default Value: N/A

Units: Percent (%)

Equation: READ_DUTY_CYCLE = Y x 2^{N}

Range: N/A

COMMAND	READ_DUTY_CYCLE (94h)															
Format	Linear-11															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	N/A															

PMBUS™ SPECIFICATIONS

READ_FREQUENCY (95h)

Definition: Reports the actual switching frequency of the converter during the enable state.

Data Length in Bytes: 2

Data Format: Linear-11

Type: Read only

Default Value: N/A

Units: KHz

Equation: READ_FREQUENCY = Y x 2^N

Range: N/A

COMMAND	READ_FREQUENCY (95h)															
Format	Linear-11															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	N/A															

PMBUS™_REVISION (98h)

Definition: The PMBus REVISION command returns the revision of the PMBus Specification to which the device is compliant.

Data Length in Bytes: 1

Data Format: Bit Field

Type: Read only

Protectable: Yes (read only)

Default Value: 33h (Part 1 Revision 1.3, Part 2 Revision 1.3)

Units: N/A

COMMAND	PMBUS_REVISION (98h)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function	See Following Table							
Default Value	0	0	1	1	0	0	1	1

BIT 7:4	RART 1 REVISION	BITS 3:0	RART 2 REVISION
0000	1.0	0000	1.0
0001	1.1	0001	1.1
0010	1.2	0010	1.2
0011	1.3	0011	1.3

PMBUS™ SPECIFICATIONS

MFR_ID (99h)

Definition: Sets a user defined identification string not to exceed 32 bytes. The sum total of characters in MFR_ID, MFR_MODEL, MFR_REVISION, MFR_LOCATION, MFR_DATE, MFR_SERIAL USER_DATA_00, USER_DATA_01, and USER_DATA_02 plus one byte per command cannot exceed 128 bytes. This limitation includes multiple writes of this command before a STORE command. To clear multiple writes, perform a RESTORE, write this command, then perform a STORE/RESTORE.

Data Length in Bytes: User defined

Data Format: ASCII, ISO/IEC 8859-1

Type: Block R/W

Protectable: Yes

Default Value: LGA110D-01DADJJ

Units: N/A

MFR_REVISION (9Bh)

Definition: Sets a user defined revision string not to exceed 32 bytes. The sum total of characters in MFR_ID, MFR_MODEL, MFR_REVISION, MFR_LOCATION, MFR_DATE, MFR_SERIAL USER_DATA_00, USER_DATA_01, and USER_DATA_02 plus one byte per command cannot exceed 128 bytes. This limitation includes multiple writes of this command before a STORE command. To clear multiple writes, perform a RESTORE, write this command, then perform a STORE/RESTORE.

Data Length in Bytes: User defined

Data Format: ASCII. ISO/IEC 8859-1

Type: Block R/W

Protectable: Yes

Default Value: 001

Units: N/A

MFR_SERIAL (9Eh)

Definition: Sets a user defined serialized identifier string not to exceed 32 bytes. The sum total of characters in MFR_ID, MFR_MODEL, MFR_REVISION, MFR_LOCATION, MFR_DATE, MFR_SERIAL USER_DATA_00, USER_DATA_01, and USER_DATA_02 plus one byte per command cannot exceed 128 bytes. This limitation includes multiple writes of this command before a STORE command. To clear multiple writes, perform a RESTORE, write this command, then perform a STORE/RESTORE.

Data Length in Bytes: User defined

Data Format: ASCII. ISO/IEC 8859-1

Type: Block R/W

Protectable: Yes

Default Value: Null

Units: N/A

PMBUS™ SPECIFICATIONS

USER_DATA_00 (B0h)

Definition: USER_DATA_00 sets a user defined data string not to exceed 32 bytes. The sum total of characters in MFR_ID, MFR_MODEL, MFR_REVISION, MFR_LOCATION, MFR_DATE, MFR_SERIAL and USER_DATA_00 plus one byte per command cannot exceed 128 bytes. This limitation includes multiple writes of this command before a STORE command. To clear multiple writes, perform a RESTORE, write this command then perform a STORE/RESTORE.

Data Length in Bytes: User defined

Data Format: ASCII. ISO/IEC 8859-1

Type: Block R/W

Protectable: Yes

Default Value: Vo1=41h, Vo2=42h

Units: N/A

USER_CONFIG (D1h)

Definition: Configures several user-level features. This command should be saved immediately to the desired user or default store after being written. This is recommended when written as an individual command or as part of a series of commands in a configuration file or script.

Data Length in Bytes: 2

Data Format: Bit Field

Type: R/W

Protectable: Yes

Default Value: 1015h/1016h Sync set by ASCRCFG pinstrap. (Min Duty 1.17%, Minimum Duty Cycle Control disable, DEM Boot Cap Refresh disable, XTEMP disabled, fault bus disabled, PG open drain, TMON Smart Power Temp Fault, TMON enabled, SYNC uses internal clock and output internal clock/external clock)

Units: N/A

COMMAND	USER_CONFIG (D1h)															
Format	Bit Field															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table															
Default Value	1	0	0	0	0	0	0	0	0	0	0	1	0	1	ASCRCFG	

PMBUS™ SPECIFICATIONS

BITS	FIELD NAME	VALUE	SETTING	DESCRIPTION
15:11	Minimum Duty Cycle	00010	0-31d	Sets the Minimum Duty Cycle in percent (%). The percentage value is defined by the following expression: Minimum Duty Cycle = 2 x (Setting+1) / 512. This feature must be enabled by setting Bit 10 to 1 (enabled).
10	Minimum Duty Cycle Enable	0	Disable	Minimum duty cycle disabled.
		1	Enable	Minimum duty cycle enabled.
9	DEM Boot Cap Refresh	0	Disable	Low-side gate minimum pulse-width disabled .
		1	Enable	Low-side gate minimum pulse-width enabled during diode emulation mode. This ensures that the top FET bootstrap capacitor is re-charged every switch cycle.
8	Not Used	0	Not Used	Not Used
7	Enable Fault Bus	0	Disable	Disable fault bus
		1	Enable	Enable fault bus
6	XTEMP/Tracking Select	0	Disable	Disable external temperature sensor. Enables TRK (tracking) input to TEMP/TRK pin.
		1	Enable	Enable external temperature sensor. Disables TRK input.
5	Power-Good Pin Configuration	0	Open Drain	0 = PG is open-drain output
		1	Push-Pull	1 = PG is push-pull output
4:3	TEMP Fault Select	00	Internal temperature sensor selected	Selects internal temperature sensor to determine temperature faults.
		01	External temperature sensor selected	Selects external temperature sensor to determine temperature faults. Bit 2 above must be set to 1 (enable XTEMP).
		10	TMON SPS temperature input selected	Selects the TMON Smart Power Stage temperature sensor input to determine temperature faults. Bit 2 must be set to 1 (enable TMON). Note: Voltages above 2.5 V on the TMON pin cause the device to automatically shut-down and latch off, regardless of the OT_FAULT_LIMIT setting when using TMON for overtemperature faults.
		11	Not Used	Not Used
2	TMON enable	0	Disable	Disable TMON input
		1	Enable	Enable TMON input
1:0	Sync Pin Configuration	00	Internal Clock	Not for application used.
		01	Use and Output Internal Clock	Use internal clock and output internal clock.
		10	External Clock	Use external clock
		11	Not Used	Not Used

PMBUS™ SPECIFICATIONS

DDC_CONFIG (D3h)

Definition: Configures DDC addressing and current sharing for up to eight phases. To operate as a 2-phase controller, set both phases (devices) to the same rail ID, set phases in rail to 2, then set each phase ID sequentially as 0 and 1. The devices automatically equally offset the phases in the rail. For example, in a 2-phase rail the phases are offset by 180°. When a device is configured to be part of a current sharing rail, DDC_GROUP must be configured so that all phases in the current sharing rail have the same DDC_GROUP ID and are set to respond to DDC_GROUP OPERATION and VOUT COMMAND messages. See the DDC_GROUP command for more details.

Data Length in Bytes: 2

Data Format: Bit Field

Type: R/W

Protectable: Yes

Default Value: PMBus address pin-strap dependent.

Units: N/A

COMMAND	DDC_CONFIG (D3h)															
Format	Bit Field															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table															
Default Value	0	0	0	Lower 5 bits of device address					0	0	0	0	0	0	0	0

BITS	FIELD NAME	VALUE	SETTING	DESCRIPTION
15:13	Phase ID	0 to 7	0	Sets the output's phase position within the rail
12:8	Rail ID	0 to 31d	0	Identifies the device as part of a current sharing rail (shared output)
7:3	Not Used	00	00	Not Used
2:0	Phases In Rail	0 to 7	0	Identifies the number of phases on the same rail (+1)

PMBUS™ SPECIFICATIONS

POWER_GOOD_DELAY (D4h)

Definition: Sets the delay applied between the output exceeding the PG threshold (POWER_GOOD_ON) and asserting the PG pin. The delay time can range from 0ms up to 125ms. POWER_GOOD may not assert if the device is enabled for less than 2 ms. Values outside of the range are not accepted.

Data Length in Bytes: 2

Data Format: Linear-11

Type: R/W

Protectable: Yes

Default Value: BA00h, 1 ms

Units: milliseconds (ms)

Equation: POWER_GOOD_DELAY = Y x 2^N

Range: 0 ms to 125 ms

COMMAND	POWER_GOOD_DELAY (D4h)															
Format	Linear-11															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	1	0	1	1	1	0	1	0	0	0	0	0	0	0	0	0

PMBUS™ SPECIFICATIONS

ASCR_ADVANCED (D5h)

Definition: Allows user configuration of advanced ASCR settings which have an impact on PWM jitter. ASCR Threshold sets the level that determines when the output voltage is considered to be at a steady state level. ASCR Threshold gain sets the ASCR gain reduction amount when the output voltage is considered to be in the steady state condition.

Data Length in Bytes: 2

Data Format: Bit Field and non-signed binary

Type: Block R/W

Protectable: Yes

Default Value: 2320h (Divide by 4, 320h threshold setting)

Units: N/A

COMMAND	ASCR_ADVANCED (D5h)															
Format	Bit Field															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Not Used						Thresh. Gain		ASCR Threshold							
Default Value	0	0	1	0	0	0	1	1	0	0	1	0	0	0	0	0

BITS	Purpose	VALUE	DESCRIPTION
15:14	Not Used	00	Not Used
13:12	ASCR Threshold Gain Select Setting	00	Divide by 1
		01	Divide by 2
		10	Divide by 4
		11	Divide by 8
11:0	ASCR Threshold Setting	0-FFFh	ASCR Threshold

PMBUS™ SPECIFICATIONS

SNAPSHOT_FAULT_MASK (D7h)

Definition: Prevents faults from causing a SNAPSHOT event (and store) from occurring.

Data Length in Bytes: 2

Data Format: BIT

Type: R/W

Protectable: Yes

Default Value: 0000h (no faults masked)

Units: N/A

Range: N/A

COMMAND	SNAPSHOT_FAULT_MASK (D7h)															
Format	Bit Field															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	See Following Table															
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BITS	STATUS BIT NAME	MEANING
15	Fault Phase	Ignore phase faults in a current sharing rail.
14	Fault Group	Ignore rail faults in a fault spreading group.
13	Fault CPU	Ignore CPU faults.
12	Fault UT	Ignore under-temperature faults.
11	Fault OT	Ignore over-temperature faults.
10	Fault Peak OC	Ignore peak output overcurrent faults.
9	Fault Peak UC	Ignore peak output undercurrent faults.
8	Fault EN Pin as Fault Bus	Ignore Enable pin faults when the Enable pin is used as a fault bus.
7	Fault VIN_OV	Ignore input overvoltage faults.
6	Fault VOUT_OV	Ignore output overvoltage faults.
5	Fault VOUT_UV	Ignore output undervoltage faults.
4	Fault SPS	Ignore Smart Power Stage (SPS) faults.
3	Fault Sync	Ignore loss of synchronization faults.
2	Fault VIN_UV	Ignore input undervoltage faults.
1	Fault IOUT_OC	Ignore output average overcurrent faults.
0	Fault IOUT_UC	Ignore output average undercurrent faults.

PMBUS™ SPECIFICATIONS

MFR_SMBALERT_MASK (DBh)

Definition: Prevents faults from activating the SALRT pin. The bits in each byte correspond to a specific fault type as defined in the STATUS command.

Data Length in Bytes: 7

Data Format: Bit Field

Type: R/W

Protectable: Yes

Default Value: 00 00 00 00 00 00 00h (No faults masked)

Units: N/A

COMMAND	MFR_SMBALT_MASK (DBh)							
Format	Bit Field							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table							
Bit Position	55	54	53	52	51	50	49	48
Default Value Byte 6	0	0	0	0	0	0	0	0
Bit Position	47	46	45	44	43	42	41	40
Default Value Byte 5	0	0	0	0	0	0	0	0
Bit Position	39	38	37	36	35	34	33	32
Default Value Byte 4	0	0	0	0	0	0	0	0
Bit Position	31	30	29	28	27	26	25	24
Default Value Byte 3	0	0	0	0	0	0	0	0
Bit Position	23	22	21	20	19	18	17	16
Default Value Byte 2	0	0	0	0	0	0	0	0
Bit Position	15	14	13	12	11	10	9	8
Default Value Byte 1	0	0	0	0	0	0	0	0
Bit Position	7	6	5	4	3	2	1	0
Default Value Byte 0	0	0	0	0	0	0	0	0

BITS	STATUS BIT NAME	MEANING
6	STATUS_MFR_SPECIFIC	Mask manufacturer specific faults as identified in the STATUS_MFR_SPECIFIC byte
5	STATUS_OTHER	Not Used
4	STATUS_CML	Mask communications, memory or logic specific faults as identified in the STATUS_CML byte
3	STATUS_TEMPERATURE	Mask temperature specific faults as identified in the STATUS_TEMPERATURE byte
2	STATUS_INPUT	Mask input specific faults as identified in the STATUS_INPUT byte
1	STATUS_IOUT	Mask output current specific faults as identified in the STATUS_IOUT byte
0	STATUS_VOUT	Mask output voltage specific faults as identified in the STATUS_VOUT byte

PMBUS™ SPECIFICATIONS

ASCR_CONFIG (DFh)

Definition: Allows user configuration of ASCR settings. ASCR Gain is analogous to bandwidth, ASCR Residual is analogous to damping. To improve load transient response performance, increase ASCR Gain. To lower transient response overshoot, increase ASCR Residual. Increasing ASCR gain can result in increased PWM jitter and should be evaluated in the application circuit. Excessive ASCR gain can lead to excessive output voltage ripple. Increasing ASCR Residual to improve transient response damping can result in slower recovery times, but does not affect the peak output voltage deviation. Typical ASCR Gain settings range from 100 to 1000, and typical ASCR Residual settings range from 10 to 90. It is recommended to set ASCR Gain to 250 and ASCR residual to 90 with recommended output capacitor in "Output Specifications" section. It is also recommended to follow "PCB Layout Guideline" for stability. If customer needs to reset the ASCR_CONFIG, customer needs to check the stability with the new ASCR_CONFIG setting base on their application. In multi-phase condition, the ASCR setting must be set the same for all phases.

Data Length in Bytes: 4

Data Format: Bit Field and non-signed binary

Type: Block R/W

Protectable: Yes

Default Value: ASCRCFG pin-strap setting (Integral Gain = 50, ASCR Residual = 90)

Units: N/A

COMMAND	ASCR_CONFIG (DFh)															
Format	Bit Field															
Bit Position	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Integral Gain								ASCR Residual							
Default Value	0	1	0	1	0	0	0	0	1	0	0	1	0	0	0	0
Format	Bit Field															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	ASCR Gain															
Default Value	ASCRCFG Pin-strap Setting (Gain)															

BITS	PURPOSE	VALUE	DESCRIPTION
31:24	Integral gain	0-7Fh	Error signal gain
23:16	ASCR Residual	0-7Fh	ASCR residual
15:0	ASCR gain	0-FFh	ASCR gain

PMBUS™ SPECIFICATIONS

SEQUENCE (E0h)

Definition: Identifies the Rail DDC ID of the prequel and sequel rails when performing multi-rail sequencing. The device enables its output when its EN or OPERATION enable state, as defined by ON_OFF_CONFIG, is set and the prequel device has issued a power-good event on the DDC bus as a result of the prequel's Power-Good (PG) signal going high. The device disables its output (using the programmed delay values) when the sequel device has issued a power-down event on the DDC bus at the completion of its ramp-down (its output voltage is 0V).

The data field is a two-byte value. The most-significant byte contains the 5-bit Rail DDC ID of the prequel device. The least-significant byte contains the 5-bit Rail DDC ID of the sequel device. The most significant bit of each byte contains the enable of the prequel or sequel mode.

Fault spreading is not automatic in devices that have a prequel or sequel. When a device shuts down due to a fault, it does not disable its output and does not send a message to its sequel or prequel to disable. If fault spreading behavior is desired, use the DDC_GROUP or LEGACY_FAULT_GROUP commands. Automatic fault retry behavior is not supported for fault spreading or sequencing groups.

A device that is tracking another device (is tracking the signal on its VTRK pin, see TRACK_CONFIG), cannot be a sequel or prequel in a sequencing group.

Data Length in Bytes: 2

Data Format: Bit Field

Type: R/W

Protectable: Yes

Default Value: 00h (prequel and sequel disabled)

Units: N/A

COMMAND	SEQUENCE (E0h)															
Format	Bit Field															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table															
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BITS	FIELD NAME	VALUE	SETTING	DESCRIPTION
15	Prequel Enable	0	Disable	Disable, no prequel preceding this rail
		1	Enable	Enable, prequel to this rail is defined by Bits 12:8
14:13	Not Used	0	Not Used	Not Used
12:8	Prequel Rail DDC ID	0-31d	DDC ID	Set to the DDC ID of the prequel rail
7	Sequel Enable	0	Disable	Disable, no sequel following this rail
		1	Enable	Enable, sequel to this rail is defined by Bits 4:0
6:5	Not Used	0	Not Used	Not Used
4:0	Sequel Rail DDC ID	0-31d	DDC ID	Set to the DDC ID of the sequel rail

PMBUS™ SPECIFICATIONS

DDC_GROUP (E2h)

Definition: Rails (output voltages) are assigned Group numbers to share specified behaviors. The DDC_GROUP command configures fault spreading group ID and enable, broadcast OPERATION group ID and enable, and broadcast VOUT_COMMAND group ID and enable. Note: DDC Groups are separate and unique from DDC Rail IDs (see “DDC_CONFIG (D3h)” section). Current sharing rails must be in the same DDC Group to respond to broadcast VOUT_COMMAND and OPERATION commands.

Devices in a current sharing rail are not required to have the same POWER_FAIL group ID. Faults are automatically spread when a device is configured to be part of a current sharing rail. If you want a current sharing rail to spread faults with another rail, then all the devices in that current sharing rail should have the same POWER_FAIL group ID as the rail it is expected to share POWER_FAIL faults with. Automatic fault retry behavior is not supported for fault spreading or sequencing groups.

When a device is set to ignore DDC_GROUP messages, the device still transmits DDC messages with its own DDC ID. Note: The default DDC_GROUP ID is set to 0d, which is a valid DDC_GROUP number, so even a device with the default setting (ignore all DDC groups, all DDC group IDs set to 0d) still transmits DDC_GROUP messages, despite ignoring DDC_GROUP messages from other devices on the DDC bus.

DDC Rail IDs should not use the same ID as DDC_GROUPS. In other words, if a device is using a DDC Rail ID of 0x02, no devices should be using GROUP_ID 0x02.

Data Length in Bytes: 4

Data Format: Bit Field

Type: R/W

Protectable: Yes

Default Value: 00000000h (DDC groups not used)

Units: N/A

COMMAND	DDC_GROUP (E2h)															
Format	Bit Field															
Bit Position	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Not Used										EN>	VOUT_COMMAND Group ID				
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Format	Bit Field															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Not Used		EN>	OPERATION Group ID					Not Used			Power Fail Group ID				
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

PMBUS™ SPECIFICATIONS

BITS	PURPOSE	VALUE	DESCRIPTION
31:22	Not Used	00	Not Used
21	BROADCAST_VOUT_COMMAND response	1	Responds to broadcast VOUT_COMMAND with same Group ID
		0	Ignores broadcast VOUT_COMMAND
20:16	BROADCAST_VOUT_COMMAND group ID	0-31d	Group ID sent as data for broadcast VOUT_COMMAND events
15:14	Not Used	00	Not Used
13	BROADCAST_OPERATION response	1	Responds to broadcast OPERATION with same Group ID
		0	Ignores broadcast OPERATION
12:8	BROADCAST_OPERATION group ID	0-31d	Group ID sent as data for broadcast OPERATION events
7:6	Not Used	00	Not Used
5	POWER_FAIL response	1	Responds to POWER_FAIL events with same Group ID
		0	Ignores POWER_FAIL events with same Group ID
4:0	POWER_FAIL group ID	0-31d	Group ID sent as data for broadcast POWER_FAIL events

PMBUS™ SPECIFICATIONS

STORE_CONTROL (E3h)

Definition: Used to store command settings in the User and Default Stores while the device is enabled. Used in conjunction with STORE_DATA.

Data Length in Bytes: 1

Data Format: Bit Field

Type: R/W

Protectable: Yes

Default Value: N/A

Units: N/A

COMMAND	STORE_CONTROL (E3h)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table							
Default Value	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A

BITS	FIELD NAME	VALUE	DESCRIPTION
7:4	Store to be read or written to	0001	User store
		0010	Default store
		0000, 0011-1111	Not used
3:0	Command	0000	Read store
		0001	Erase store
		0010	Start write
		0011	End write
		0100-1111	Not used

PMBUS™ SPECIFICATIONS

MFR_IOUT_OC_FAULT_RESPONSE (E5h)

Definition: Configures the IOUT overcurrent fault response as defined by the table below. The command format is the same as the PMBus standard fault responses except that it sets the overcurrent status bit in STATUS_IOUT. The delay time is the time between fault detected and restart attempts. It's highly recommended set as default "no retry" qualified only.

Data Length in Bytes: 1

Data Format: Bit Field

Type: R/W

Protectable: Yes

Default Value: CFG pin-strap setting

Units: Retry time unit = 35 ms

COMMAND	MFR_IOUT_OC_FAULT_RESPONSE (E5h)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table							
Default Value	CFG Pin-strap Setting							

BITS	FIELD NAME	VALUE	DESCRIPTION
7:6	Response behavior, for all modes, the device: • Pulls SALRT low • Sets the related fault bit in the status registers. Fault bits are only cleared by the CLEAR_FAULTS command.	00	Not used
		01	Not used
		10	Disable without delay and retry according to the setting in Bits 5:3.
		11	Not used
5:3	Retry Setting	000	No retry. The output remains disabled until the fault is cleared.
		001-111	Attempts to restart continuously, without checking if the fault is still present, until it is commanded OFF (by the CONTROL pin or OPERATION command or both), bias power is removed, or another fault condition causes the unit to shut down. The time between the start of each attempt to restart is set by the value in Bits 2:0.
2:0	Retry Delay	000-111	Retry delay time = (Value +1)*35 ms. Sets the time between retries in 35 ms increments. Range is 35 ms to 280 ms.

PMBUS™ SPECIFICATIONS

MFR_IOUT_UC_FAULT_RESPONSE (E6h)

Definition: Configures the IOUT undercurrent fault response as defined by the table below. The command format is the same as the PMBus standard fault responses except that it sets the undercurrent status bit in STATUS_IOUT. The delay time is the time between fault detected and restart attempts. It's highly recommended set as default "no retry" qualified only.

Data Length in Bytes: 1

Data Format: Bit Field

Type: R/W

Protectable: Yes

Default Value: CFG pin-strap setting

Units: Retry time unit = 35ms

COMMAND	MFR_IOUT_UC_FAULT_RESPONSE (E6h)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table							
Default Value	CFG Pin-strap Setting							

BITS	FIELD NAME	VALUE	DESCRIPTION
7:6	Response behavior, for all modes, the device: • Pulls SALRT low • Sets the related fault bit in the status registers. Fault bits are only cleared by the CLEAR_FAULTS command.	00	Not used
		01	Not used
		10	Disable without delay and retry according to the setting in Bits 5:3.
		11	Not used
5:3	Retry Setting	000	No retry. The output remains disabled until the fault is cleared.
		001-111	Attempts to restart continuously, without checking if the fault is still present, until it is commanded OFF (by the CONTROL pin or OPERATION command or both), bias power is removed, or another fault condition causes the unit to shut down. The time between the start of each attempt to restart is set by the value in Bits 2:0.
2:0	Retry Delay	000-111	Retry delay time = (Value +1)*35 ms. Sets the time between retries in 35ms increments. Range is 35 ms to 280 ms.

PMBUS™ SPECIFICATIONS

IOUT_AVG_OC_FAULT_LIMIT (E7h)

Definition: Sets the IOUT average overcurrent fault threshold. For down-slope sensing, this corresponds to the average of all the current samples taken during the (1-D) time interval, excluding the current sense blanking time (which occurs at the beginning of the 1-D interval). For up-slope sensing, this corresponds to the average of all the current samples taken during the D time interval, excluding the current sense blanking time (which occurs at the beginning of the D interval). This feature shares the OC fault bit operation (in STATUS_IOUT) and OC fault response with IOUT_ OC_FAULT_LIMIT. Values outside of the range are not accepted.

Data Length in Bytes: 2

Data Format: Linear-11

Type: R/W

Protectable: Yes

Default Value: 0.8 x (IOUT_OC_FAULT_LIMIT pin-strap setting - 5)

Units: A

Equation: IOUT_AVG_OC_FAULT_LIMIT = Y x 2^N

Range: 0 A to 100 A

COMMAND	IOUT_AVG_OC_FAULT_LIMIT (E7h)															
Format	Linear-11															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	0.8 x (IOUT_OC_FAULT_LIMIT pin-strap setting - 5)															

PMBUS™ SPECIFICATIONS

ADVANCED_CONFIG (E9h)

Definition: Sets the PWM mid-drive voltage, SMBus I/O voltage and enables/disables the VG LDO.

Data Length in Bytes: 1

Data Format: Bit Field

Type: R/W

Protectable: Yes

Default Value: 01h

COMMAND	USER_GLOBAL_CONFIG (E9h)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	Reserved					R/W	R/W	R/W
Function	See Following Table							
Default Value	N/A	N/A	N/A	N/A	N/A	0	0	1

BITS	FIELD NAME	VALUE	DESCRIPTION
7:3	Reserved	N/A	Reserved
2	vgDisable	0	1 = disable, 0 = enable
1	pmbusVolt	0	0 sets V_{IN} = 2 V, V_{IL} = 0.8V for 5 V/3.3 V logic compatible 1 sets V_{IN} = 1.17 V, V_{IL} = 0.552 V for 1.8 V logic compatible
0	midDrvVolt	1	1 sets PWM mid-drive voltage to 1.5 V 0 sets PWM mid-drive voltage to 2.5 V

PMBUS™ SPECIFICATIONS

SNAPSHOT (EAh)

Definition: A 32-byte read-back of parametric and status values. It allows monitoring and status data to be stored to flash either during a fault condition or through a system-defined time using the SNAPSHOT_CONTROL command. Snapshot is continuously updated in RAM and can be read using the SNAPSHOT command. When a fault occurs, the latest snapshot in RAM is stored to flash. Snapshot data can read back by writing a 01h to the SNAPSHOT_CONTROL command, then reading SNAPSHOT.

Data Length in Bytes: 32

Data Format: Bit Field

Type: Block Read

Protectable: Yes (read only)

Default Value: N/A

Units: N/A

BITS	VALUE	PMBus COMMAND	FORMAT
31:30	Duty Cycle	READ_DUTY_CYCLE (94h)	2 Byte Linear-11
29:28	Switching Frequency	READ_FREQUENCY (95h)	2 Byte Linear-11
27:26	External Temperature 2 (TMON)	READ_TEMPERATURE_3 (8Fh)	2 Byte Linear-11
25:24	External Temperature 1	READ_TEMPERATURE_2 (8Eh)	2 Byte Linear-11
23:22	Internal Temperature	READ_TEMPERATURE_1 (8Dh)	2 Byte Linear-11
21	Manufacturer Specific Status Byte	STATUS_MFR_SPECIFIC (80h)	1 Byte Bit Field
20	CML Status Byte	STATUS_CML (7Eh)	1 Byte Bit Field
19	Temperature Status Byte	STATUS_TEMPERATURE (7Dh)	1 Byte Bit Field
18	Input Status Byte	STATUS_INPUT (7Ch)	1 Byte Bit Field
17	IOUT Status Byte	STATUS_IOUT (7Bh)	1 Byte Bit Field
16	VOUT Status Byte	STATUS_VOUT (7Ah)	1 Byte Bit Field
15:14	Highest Measured Output Current	N/A (Peak measured output current)	2 Byte Linear-11
13:12	Output Current	READ_IOUT (8Ch)	2 Byte Linear-11
11:10	Output Voltage	READ_VOUT (8Bh)	2 Byte Linear-16 Unsigned
9:8	Input Voltage	READ_VIN (88h)	2 Byte Linear-11
7:6	All Faults	N/A	2 Byte Bit Field
5	First Fault	N/A	1 Byte Bit Field
4:1	Uptime	N/A	4 Byte Integer
0	Flash Memory Status Byte	N/A	1 Byte Bit Field

PMBUS™ SPECIFICATIONS

FIRST FAULT		
BITS	**STATUS BIT NAME**	**MEANING**
7:4	Not Used	Not Used
3	IOUT_PEAK_OC	Peak output overcurrent was the first fault.
2	IOUT_AVG_OC	Average output overcurrent was the first fault.
1	VOUT_OV	Output overvoltage was the first fault.
0	VIN_UV	Input undervoltage was the first fault.

ALL FAULTS		
BITS	**STATUS BIT NAME**	**MEANING**
15	Fault Phase	A DDC rail fault occurred.
14	Fault Group	A DDC group fault occurred.
13	Fault CPU	A CPU fault occurred.
12	Fault UT	An under-temperature fault occurred.
11	Fault OT	An over-temperature fault occurred.
10	Fault Peak OC	A peak output overcurrent fault occurred.
9	Fault Peak UC	A peak output undercurrent fault occurred.
8	Fault EN Pin as Fault Bus	The EN pin was pulled low in response to a fault.
7	Fault VIN_OV	An input overvoltage fault occurred.
6	Fault VOUT_OV	An output overvoltage fault occurred.
5	Fault VOUT_UV	An output undervoltage fault occurred.
4	Fault SPS	A MOSFET driver fault occurred.
3	Fault Sync	A loss of clock synchronization fault occurred.
2	Fault VIN_UV	An input undervoltage fault occurred.
1	Fault IOUT_OC	An average output overcurrent fault occurred.
0	Fault IOUT_UC	An average output undercurrent fault occurred.

PMBUS™ SPECIFICATIONS

LEGACY_FAULT_GROUP (F0h)

Definition: Allows the LGA110D to sequence and fault spread with devices. This command sets which rail DDC IDs should be listened to for fault spreading information. The data sent is a 4-byte, 32-bit vector in which every bit represents a rail's DDC ID. A bit set to 1 indicates a device DDC ID to which the configured device responds upon receiving a fault spreading event. In this vector, Bit 0 of Byte 0 corresponds to the rail with DDC ID 0. Following through, Bit 7 of Byte 3 corresponds to the rail with DDC ID 31.

Note: The device/rail's own DDC ID should not be set within the LEGACY_FAULT_GROUP command for that device/rail.

All devices in a current share rail must shut down for the rail to report a shutdown. If fault spread mode is enabled in DDC_CONFIG, the device immediately shuts down if one of its DDC_GROUP members fail. The device/rail does not attempt its configured fault restart (retry).

If fault spread mode is disabled in DDC_CONFIG, the device immediately shuts down (not sequenced). The rails/devices in a sequencing set do not attempt their configured fault restart (retry). If fault spread mode is disabled and sequencing is also disabled, the device ignores faults from other devices and stays enabled.

Data Length in Bytes: 4

Data Format: Bit field

Type: Block R/W

Protectable: Yes

Default Value: 00000000h (no fault spreading with legacy devices)

Units: N/A

COMMAND	LEGACY_FAULT_GROUP (F0h)															
Format	Bit Field															
Bit Position	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table															
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Format	Bit Field															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table															
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BITS	PURPOSE	VALUE	SETTING	DESCRIPTION
31:0	Fault Group	N/A	00000000h	Identifies the devices in the fault spreading group.

PMBUS™ SPECIFICATIONS

STORE_DATA (F2h)

Definition: Stores the command settings in the User and/or Default stores while the device is enabled. Used in conjunction with STORE_CONTROL (E3h). This command indicates to the device that the next 4 bytes are PMBus command codes and/or data. STORE_DATA commands, along with their 4 bytes of data, are repeatedly sent to the device until all configuration commands and data have been sent to the device. If the data that needs to be sent results in a STORE_DATA command that would have less than 4 bytes, the unused bytes should be filled with FFh.

Note: These filler bytes are used when the CRC is calculated.

Data Length in Bytes: 4

Data Format: Custom

Type: R/W

Protectable: Yes

Default Value: N/A

Units: N/A

PMBUS™ SPECIFICATIONS

SNAPSHOT_CONTROL (F3h)

Definition: Controls, configures, and erases SNAPSHOT data. As shown in the following table, this command is used to arm and disarm SNAPSHOT, report back the number of SNAPSHOT data record locations that are available for new data, select the data record to read back, specify whether a single or multiple SNAPSHOT should be taken after a device is disabled, if a SNAPSHOT can only be taken when the device is enabled, enabling and disabling SNAPSHOT_CONTROL, and erasing all SNAPSHOT data.

The Erase All bit must be sent as a separate command. All other bits are ignored when the Erase All bit is sent. For example, 0000 0000 0000 0010b and 1111 1111 1111 1111b both (only) erase all SNAPSHOT data. The hose must wait at least 20ms before issuing any other PMBus commands after writing the Erase All bit.

Data Length in Bytes: 2

Data Format: Bit Field

Type: R/W

Protectable: Yes

Default Value: 0800h

Units: N/A

COMMAND	SNAPSHOT_CONTROL (F3h)															
Format	Bit Field															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table															
Default Value	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0

BITS	FIELD NAME	VALUE	SETTING	DESCRIPTION
15	SNAPSHOT Armed	0	Disabled	Not Armed
		1	Enabled	Armed. SNAPSHOT will happen on next fault (if it is not masked).
14:12	Not Used	000	Not used	Not Used
11:8	Available SNAPSHOTs Remaining	0000-1000	N/A	Number of 8 byte SNAPSHOT records available.
7	One Time	0	Disabled	SNAPSHOT will be taken whenever a fault occurs.
		1	Enabled	One SNAPSHOT will be taken when a fault occurs. Another SNAPSHOT will not be taken until the device has been disabled.
6	After Enable	0	Disabled	SNAPSHOT may be taken at any time.
		1	Enabled	SNAPSHOT will be taken only when the device is enabled (“turned on”).
5	Not Used	0	Not used	Not Used
4:2	Read Location	000-111	N/A	Specifies which SNAPSHOT data record to return when the SNAPSHOT command is read.
1	Erase All	1	(Write only)	Erases all SNAPSHOT data. This will cause Available Snapshots Remaining to become 8 (1000d) THIS BIT MUST BE SENT AS A SEPARATE COMMAND; that is, not combined with other bit settings.
0	Enable	0	Disabled	Disables SNAPSHOT_CONTROL.
		1	Enabled	Enables SNAPSHOT_CONTROL.

PMBUS™ SPECIFICATIONS

RESTORE_FACTORY (F4h)

Definition: Restores the device to the hard-coded factory default values and pin-strap definitions. The device retains the Default and User stores for restoring.

Data Length in Bytes: N/A

Data Format: N/A

Type: Write only

Protectable: Yes

Default Value: N/A

Units: N/A

PINSTRAP_READ_STATUS (F5h)

Definition: A 5-byte read-back of an index from 0 - 31 that corresponds to the resistor value for the designated pinstrap position.

Data Length in Bytes: 5

Data Format: Bit Field

Type: Block Read

Protectable: Yes (read only)

Default Value: N/A

Units: N/A

BYTE	VALUE	FORMAT
Byte 4	CFG Resistor	8-bit Integer
Byte 3	ASCRCFG Resistor	8-bit Integer
Byte 2	SYNC Resistor Index	8-bit Integer
Byte 1	Factory Mode	8-bit Integer
Byte 0 Bits 7:4	VSET/SA VSET Resistor Index	4-bit Integer
Byte 0 Bits 3:0	VSET/SA Address Resistor Index	4-bit Integer

PMBUS™ SPECIFICATIONS

IIN_CAL_OFFSET (F6h)

Definition: Used to account for input current that is consumed by bias currents which would not be consumed by the power supply's power train.

Data Length in Bytes: 2

Data Format: Linear-11

Type: R/W

Protectable: Yes

Default Value: 8BD7h (0.03 A)

Units: A

Equation: IIN_OFFSET = Y x 2^N

Range: -10 A to 10 A

COMMAND	IIN_OFFSET (F6h)															
Format	Linear-11															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	1	0	0	0	1	0	1	1	1	1	0	1	0	1	1	1

PMBUS™ SPECIFICATIONS

SECURITY_CONTROL (FAh)

Definition: Used to read-back the security status of the User and Default stores, clear protection status of non-password protected commands, and enable the automatic command protection mode (Auto Protect Mode). SECURITY_CONTROL is used along with the PASSWORD and WRITE_PROTECT commands to allow the user to disallow changes to selected commands.

Data Length in Bytes: 1

Data Format: Bit

Type: R/W

Protectable: No

Default Value: 01h

Units: N/A

COMMAND	SECURITY_CONTROL (FAh)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	Read	Read	Read	Read	Read	R/W	R/W	R/W
Function	See Following Table							
Default Value	0	0	0	0	0	0	0	1

BITS	FIELD NAME	VALUE	DESCRIPTION
7:6	Not used	00	Not used
5	Default store protected	0	1 indicates that the Default store is protected
4	User store protected	0	1 indicates that the User store is protected
3:2	Not used	00	Not used
1	Clear protected	0	Writing a “1” clears all protected commands except the commands that are password protected
0	Auto protect	0	Writing a “1” enables auto protection mode

LGA110D set security level to 1 that protect default settings via a password.

User can save their settings in User store via PMBus command STORE_USER_ALL that is in effect on LGA110D.

User cannot overwrite default settings without correct password.

User can restore to default settings via send below PMBus commands one by one, after recycle Vin, LGA110D settings are back to default settings.

1. PRIVATE_PASSWORD (send null string 0000000000000000h)
2. RESTORE_FACTORY
3. PRIVATE_PASSWORD (send null string 0000000000000000h)
4. STORE_USER_ALL
5. Recycle Vin

PMBUS™ SPECIFICATIONS

PASSWORD (FBh)

Definition: Sets the password string for the User and Default stores. The User and Default stores can have unique passwords. The initial (default) password for both stores is null (9 bytes of zeros in hexadecimal format - not 9 ASCII “0” characters). The Default store password has priority over the User store password; that is, when the Default store password is written, protected commands in both the Default and User stores can be written to.

Data Length in Bytes: 9

Data Format: ASCII. ISO/IEC 8859-1

Type: Block Write

Protectable: No

Default Value: 000000000000000000h (null)

Units: N/A

WRITE_PROTECT (FDh)

Definition: Sets a 256-bit (32-byte) parameter which identifies which commands are to be protected against write-access. Each bit in this parameter corresponds to a command according to the command’s code. The command with a code of 00h (PAGE - not used in this device) is protected by the least-significant bit of the least-significant byte, followed by the command with a code of 01h and so forth.

Note: All possible commands have a corresponding bit regardless of whether they are can be protected or are supported by the device. Setting a command’s WRITE_PROTECT bit to “1” indicates that write-access to that command is allowed only if the appropriate password has been written to the device.

Note: The User and Default stores have unique passwords, and that writing the Default store password allows changes to both the User and Default stores.

Data Length in Bytes: 32

Data Format: Custom

Type: Block R/W

Protectable: Yes

Default Value: 00..00h

Units: N/A

APPLICATION NOTES

Typical Applications

The LGA110D has a lot of applications. Below are some typical applications:

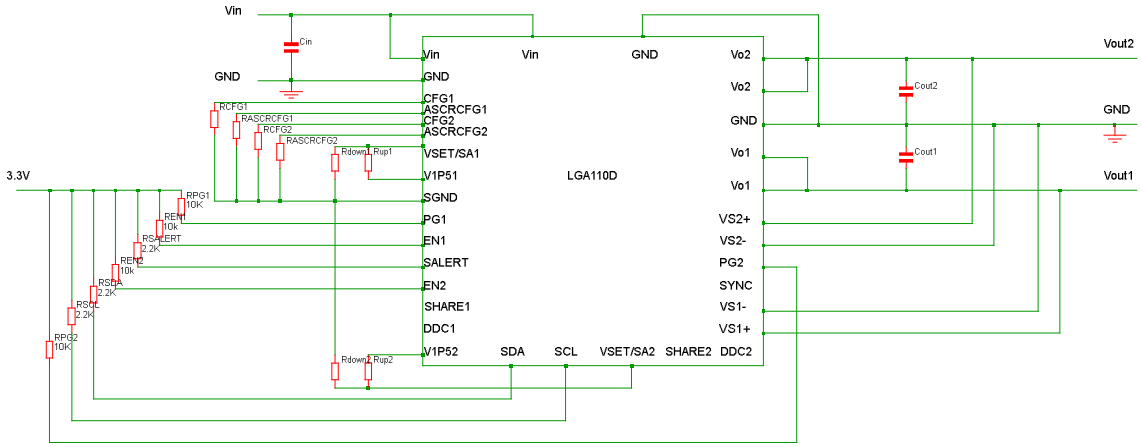


Figure 48: One module two outputs configuration

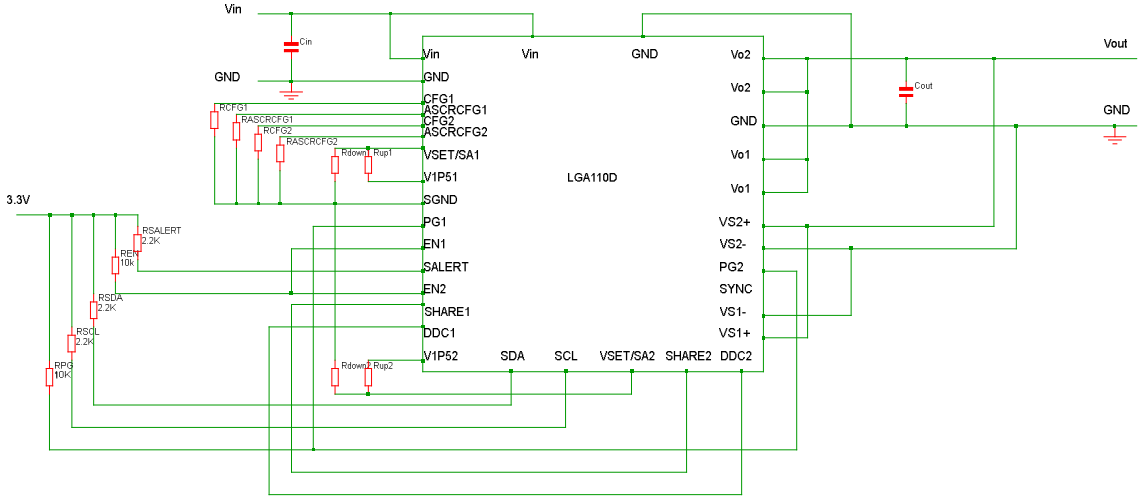


Figure 49: One module one output configuration

APPLICATION NOTES

Typical Applications

The LGA110D has a lot of applications. Below are some typical applications:

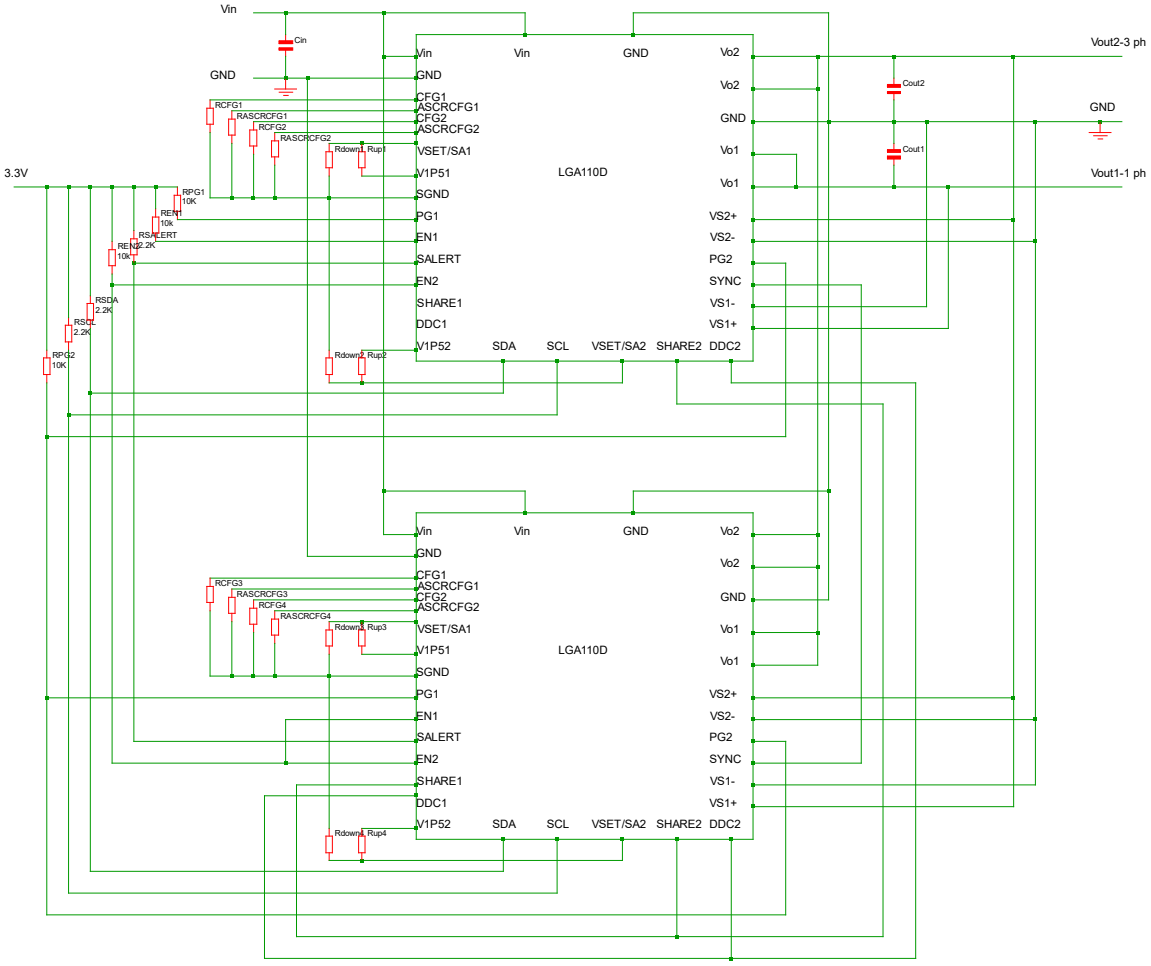


Figure 50: Two modules, 3-phase single output + 1-phase single output configuration

APPLICATION NOTES

Typical Applications

The LGA110D has a lot of applications. Below are some typical applications:

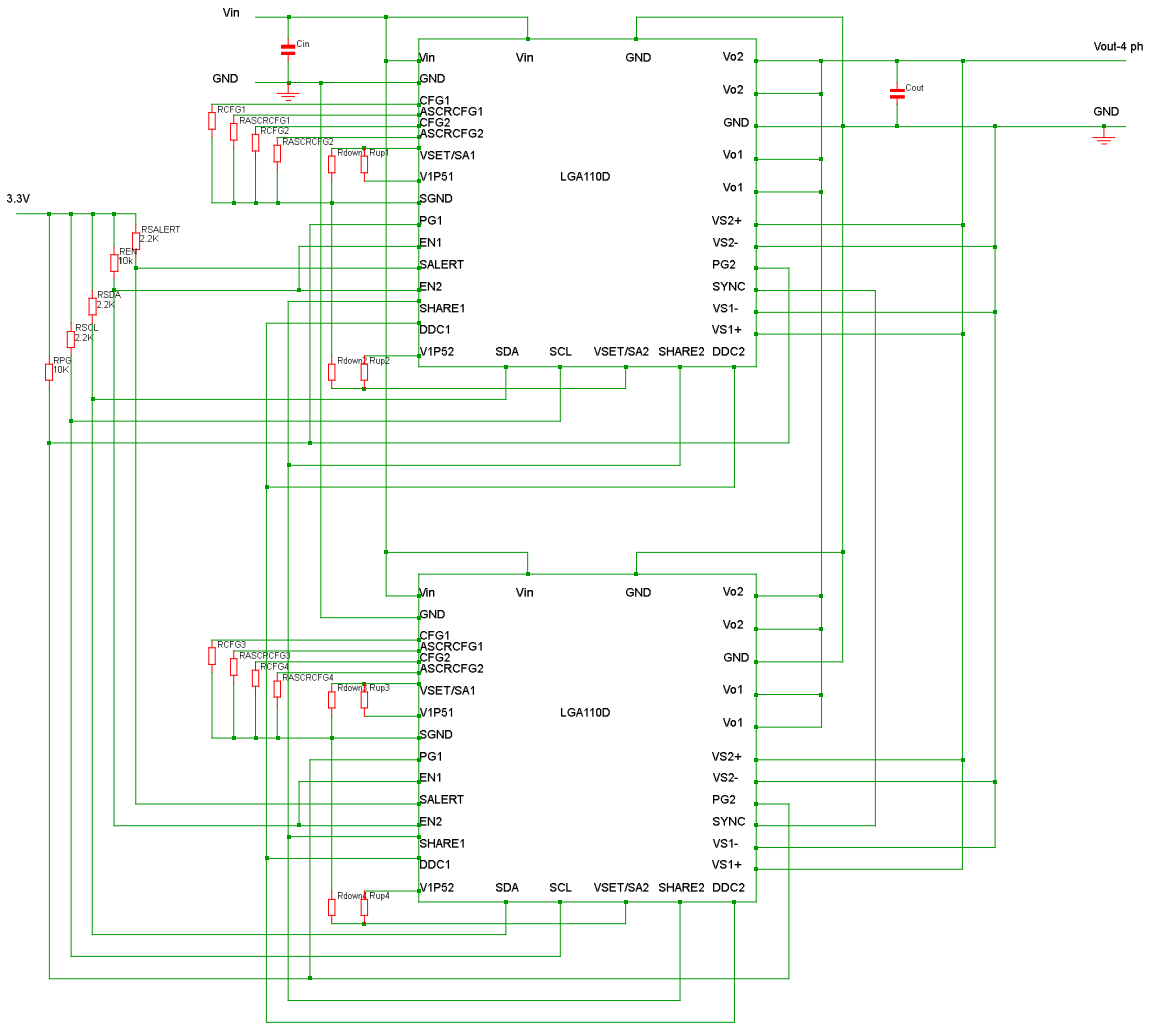
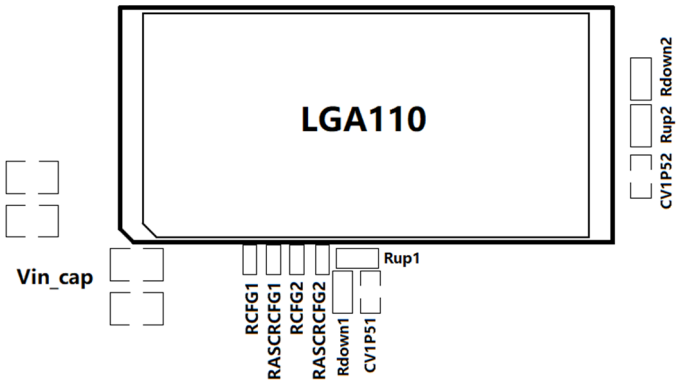


Figure 51: Two modules, 4-phase single output configuration

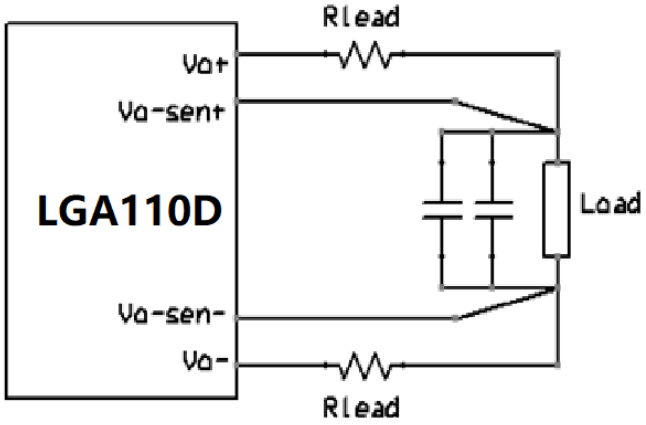
APPLICATION NOTES

PCB Layout Guideline

1. All the pin strapped resistors, Rup, Rdown, RASCRCFG, RCFG should be placed as close to the LGA110D module pins as possible to minimize loops that may pick up noise. It is recommended the path including the resistor body should less than 10mm.



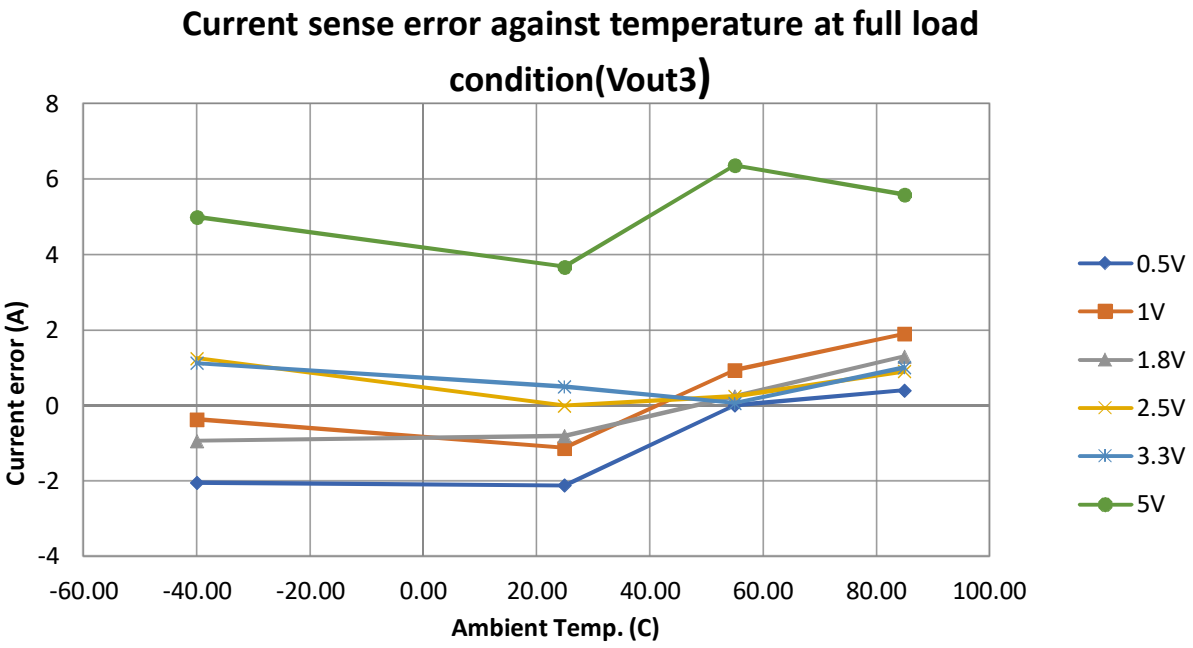
2. The output capacitors should be placed as close to the LGA110D module pins as possible to minimize the output impedance. The output capacitors should also be placed close to the remote sense point for stability.
3. The input ceramic capacitors should be placed as close to the LGA110D module pins as possible to decouple noise.
4. The LGA110D POL modules should be placed closely to the ASIC for better performance. Since the overshoot voltage during step is followed V = L*di/dt, the L is the PCB power trace inductance, if PCB impedance is high, the overshoot voltage may be high.
5. Remote sense VS+, VS- traces should be in paralleled connect to output, the traces are shield by GND to minimized noise couple. Recommended connect VS+/VS- to one high capacitance output capacitor's soldering pads that is close to actual load, please do not connect VS+/VS- very close to LGA110D output pins that is high ripple noise cause control loop unstable.



6. Full hole vias are very helpful for lower impedance and better thermal conductivity. Recommended add 28pcs full hole vias on each power pin soldering pad if possible, such as V_{IN}, V_O, GND. Recommended add 8pcs full hole vias on each soldering pad of output polymer Tan capacitor, add 4pcs full hole vias on each soldering pad of output ceramic capacitor. Even for signal pins, more full hole vias on soldering pads shall improve thermal conductivity that cool down the LGA110D module as well.

APPLICATION NOTES

Current Sense Error Against Temperature at Full Load - 2 Phases Single Output



Note: Switching frequency at 0.5 V to 5 V = 500 KHz

APPLICATION NOTES

Output Voltage and Address Set

To simplify circuit design, the LGA110D incorporates pin-strap pins that use a patented pin reader algorithm. This feature allows you to easily configure many aspects of the device. When power is applied to the LGA110D, the IC reads the values of the pin-strap resistors and configures the IC accordingly. Each resistor value corresponds to a specific configuration setting. Values not listed as configuration resistor values should not be used. Resistors with a 1% tolerance must be used.

The output voltage is adjustable from 0.5V to 5.0V. The outputs can be adjusted with the external resistors Rup and Rdown placed between the "V1P5" to "VSET/SA" and "VSET/SA" to "GND" pin (shown Figure 52). V_O1 and V_O2 can also be set by PMBus™ command. VOUT_MAX is also determined by this pin-strap setting, and is 15% greater than the Vtrim0 and Vtrim1 voltage settings by default, however VOUT_MAX can be changed via the PMBus™.

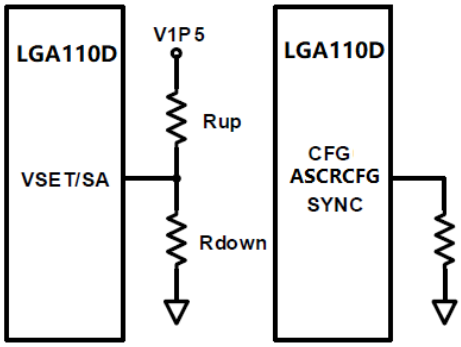


Figure 52: Output Voltage Adjustment

When communicating with multiple SMBus devices using the SMBus interface, each device must have its own unique address so the host can distinguish between the devices. The device address can be set according to the pin-strap options listed in below table.

V_O (V)	Address 0x68		Address 0x69		Address 0x6A		Address 0x6B		Address 0x6C		Address 0x6D		Address 0x6E		Address 0x6F	
	Rup (Kohm)	Rdown (Kohm)	Rup (Kohm)	Rdown (Kohm)	Rup (Kohm)	Rdown (Kohm)	Rup (Kohm)	Rdown (Kohm)	Rup (Kohm)	Rdown (Kohm)	Rup (Kohm)	Rdown (Kohm)	Rup (Kohm)	Rdown (Kohm)	Rup (Kohm)	Rdown (Kohm)
0.5	32.4	3.16	93.10	9.09	158	15.8	232	22.6	309	30.1	392	38.3	475	47.5	576	57.6
0.6	20.5	3.40	59.0	9.76	100	16.5	147	24.3	196	32.4	249	41.2	301	49.9	365	60.4
0.65	15.0	3.57	43.2	10.5	73.2	17.8	107	25.5	143	34.0	182	44.2	221	53.6	267	64.9
0.7	11.8	3.83	34.0	11.0	57.6	18.7	84.5	27.4	113	36.5	143	46.4	178	57.6	215	69.8
0.8	9.76	4.12	28.0	11.8	47.5	20.0	69.8	29.4	93.1	39.2	118	49.9	143	60.4	174	73.2
0.85	8.25	4.42	23.7	12.7	41.2	22.1	59.0	31.6	78.7	42.2	100	53.6	124	66.5	150	80.6
0.9	7.32	4.87	21.0	14.0	34.8	23.2	52.3	34.8	69.8	46.4	88.7	59.0	107	71.5	130	86.6
1.0	6.49	5.36	18.2	15.0	31.6	26.1	45.3	37.4	60.4	49.9	76.8	63.4	95.3	78.7	115	95.3
1.05	5.76	5.90	16.5	16.9	28.0	28.7	41.2	42.2	54.9	56.2	69.8	71.5	84.5	86.6	100	102
1.1	5.11	6.49	14.7	18.7	25.5	32.4	36.5	46.4	49.9	63.4	63.4	80.6	76.8	97.6	93.1	118
1.2	4.87	7.68	13.7	21.5	23.2	36.5	33.2	52.3	45.3	71.5	57.6	90.9	69.8	110	84.5	133
1.5	4.42	8.66	12.4	24.3	21.5	42.2	30.9	60.4	42.2	82.5	53.6	105	64.9	127	78.7	154
1.8	4.12	10.2	11.5	28.7	20.0	49.9	28.7	71.5	39.2	97.6	49.9	124	60.4	150	73.2	182
2.5	3.92	12.7	11.0	35.7	19.1	61.9	26.7	86.6	35.7	118	47.5	154	57.6	187	68.1	221
3.3	3.57	16.2	10.0	45.2	17.4	78.7	25.5	115	34.0	154	42.2	191	52.3	237	63.4	287
5	3.32	22.1	9.53	63.4	16.2	110	23.7	158	31.6	210	40.2	267	49.9	332	60.4	402

APPLICATION NOTES

EN

Use the Enable pin (EN) to enable and disable the LGA110D. Drive the EN pin low whenever a configuration file or script is used to configure the LGA110D, or a PMBus command is sent that could potentially damage the application circuit. When the LGA110D is used in a self-enabled mode, for example, when EN is tied to 5 V, or to a resistor divider from V_{IN}, consider the LGA110D's default factory settings. When a configuration file is used to configure the LGA110D, the factory default settings are restored to both the User and Default stores to set the device to an initialized state. Because the default state of the LGA110D is to be enabled when the EN pin is high, the LGA110D can be enabled while the PMBus commands are sent to the device during the configuration process.

The EN pin is edge triggered to achieve fast turn-off times. As a result, minimum Enable high and Enable low pulse-widths must be observed to ensure correct operation. The minimum high and low pulse widths are dependent on the configured rise, fall, and delay times and can be calculated using Equations 1 and 2:

EN low → TOFF_DELAY + TOFF_FALL + 10.5 ms (EQ. 1)

EN high → TON_DELAY + TON_RISE + POWER_GOOD_DELAY + 5.5 ms (EQ. 2)

EN low and EN high times shorter than these minimums may result in the device not responding to the trailing edge of the pulse. For example, an EN low pulse below the EN low minimum pulse width may stay in the OFF state until a valid EN low pulse is applied to the EN pin.

The EN pin can be configured for fast fault-spreading through the USER_CONFIG (D1h) command. For example, in current sharing applications, the EN pins of the devices in the current sharing rail can be tied together, and can be configured for fault-spreading. When one device detects fault condition, it can disable other devices that are connected to the same EN bus. When used in this manner, there is 20 us typical delay time for fault response. In the event of a fault, the EN pin is pulled down internally. As such, a pull-up resistor must be used for the EN bus.

Power Good

The LGA110D provides a Power-Good signal (PG) that indicates the output voltage is within a specified tolerance of its target level and no fault condition exists. By default, the PG pin asserts if the output is within 10% of the target voltage. These limits and the configuration of the pin can be changed using the POWER_GOOD_ON (5Eh) and USER_CONFIG (D1h) commands.

A PG delay period is defined as the time from when all conditions within the LGA110D for asserting PG are met to when the PG pin is actually asserted. This feature is commonly used instead of using an external reset controller to control external digital logic. By default, the LGA110D PG delay is set equal to 1ms. Set the PG delay using the PMBus command as described in POWER_GOOD_DELAY (D4h).

Digital Bus (DDC)

The Digital-DC Communications (DDC) bus communicates between LGA110D modules, and within the LGA110D itself. This dedicated bus provides the communication channel between devices for features such as sequencing, and fault spreading. The DDC pin on all Digital-DC devices that utilize sequencing, fault spreading, or current sharing must be connected together.

Stackable

When multiple point-of-load converters share a common DC input supply, adjust the clock phase offset of each device so that not all devices have coincident rising edges. Set each converter to start its switching cycle at a different point in time to dramatically reduce input capacitance requirements. Because the peak current drawn from the input supply is effectively spread out over a period of time, the peak current drawn at any given moment is reduced and the power losses proportional to I_{RMS}^2 are reduced.

To enable phase spreading, all converters must be synchronized to the same switching clock. Configuring the SYNC pin is described in “Power and Control Signal Descriptions” part. The phase offset of each device can also be set to any value between 22.5^O and 360^O in 22.5^O increments using the INTERLEAVE (37h) PMBus command.

User can set multi-phases configuration either by Artesyn GUI or PMBus commands. Please contact Artesyn to get multi-phases setting instruction.

APPLICATION NOTES

Fault Spreading

Digital-DC devices can be configured to broadcast a fault event over the DDC bus to the other devices in the group. When a fault occurs and the device is configured to shut down on a fault, the device shuts down and broadcasts the fault event over the DDC bus. The other devices on the DDC bus shut down together if configured to do so, and they attempt to restart in their prescribed order if configured to do so.

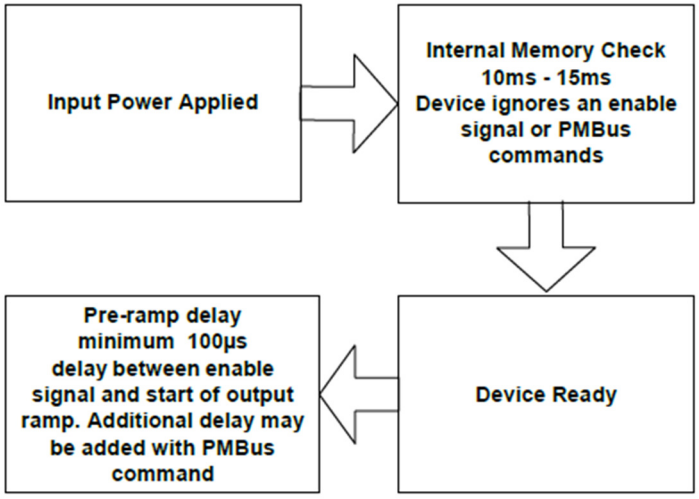
Active Current Sharing

Up to eight LGA110D devices can be paralleled together for current sharing operation. The device outputs share the current equally within a few percent, assuming all external sensing element variations and tolerances are negligible.

Start-up and Shut-down Delay Characteristics

Start-Up Procedure

The LGA110D follows a specific internal start-up procedure after power is applied to the input pin, as shown in below Figure.



Internal Startup Procedure

The device requires approximately 10-15ms to check for specific values stored in its internal memory. If you have stored values in memory, those values are loaded. When this process is completed, the device is ready to accept commands through the serial interface and the device is ready to be enabled. If the device is synchronizing to an external clock source, the clock frequency must be stable before asserting the EN pin. When enabled, the device requires approximately 100us before its output voltage is allowed to start its ramp-up process.

After the Ton-delay period expires, the output begins to ramp towards its target voltage according to the preconfigured Ton-rise time.

V_{IN} should be above the VIN_UV_FAULT_LIMIT (59h) of the LGA110D before the Enable pin is driven high.

Following this sequence will result in the most consistent turn-on delays. If a configuration file is needed to ensure proper circuit operation (when V_{IN} is first applied to the LGA110D, for example) during initial PCB turn-on and test, the Enable pin must be driven low by some means until the LGA110D configuration file is loaded. If the Enable pin is not held low, then the LGA110D may attempt to turn on with incorrect configuration settings, possibly causing circuit failure. In those cases in which a configuration file is needed to ensure proper circuit operation and the Enable pin shall be held low during the initial application of power.

APPLICATION NOTES

Ton-Delay and Rise Times

The default Ton-delay for the LGA110D in 2 O/P configuration on LGA110D is

EN1 0 ms

EN2 0 ms

TON_RISE (61h) is initially set to 3ms and TOFF_FALL (65h) is initially set to 5ms. TON_DELAY (60h) and TOFF_DELAY (64h) are initially set to 0 ms. In some applications, it may be necessary to set a delay from when an enable signal is received until the output voltage starts to ramp to its target value. In addition, the customer may wish to precisely set the time required for Vout to ramp to its target value after the delay period expires. These features can be used as part of an overall inrush current management strategy or to precisely control how fast a load IC is turned on. The LGA110D has several options for precisely and independently controlling both the delay and ramp time periods.

The Ton-delay time begins when the EN pin is asserted. Set the Ton-delay time using the PMBus command TON_DELAY (60h).

The Ton-rise time enables a precisely controlled ramp to the nominal Vout value that begins when the Ton-delay time expires. The ramp-up is monotonic and its slope can be precisely set using the PMBus command TON_RISE.

The Ton-delay and Ton-rise times can be set using PMBus commands TON_DELAY (60h) and TON_RISE (61h) over the serial bus interface. When the Ton-delay time is set to 0 ms, the device begins its ramp after the internal circuitry has initialized, which takes approximately 100 us to complete. The Ton-rise time can be set to values less than 125 ms; however, the Ton-rise time should be set to a value greater than 500 us to prevent inadvertent fault conditions due to excessive inrush current. A lower Ton-rise time limit can be estimated using the formula:

Ton-rise = C_O*V_O/I_{LIMIT}, where C_O is the total output capacitance, V_O is the output voltage, and I_{LIMIT} is the current limit setting for the LGA110D.

When using interdevice current sharing, the TON_DELAY and the TON_RISE times of each device in the same current sharing rail must be set to the same values.

Toff-Delay

During the shut-down of the converter, the controller doesn't need to wait for the preparation of the reference ramp. The propagation delay from Enable signal to PWM off is very small, and Vout can almost follow the Toff-delay setting to turn off the output. However, note that the controller is not able to ensure whether it reads EN1 status or EN2 status first, and therefore if the unit is used in 2 outputs configuration, there will be a delay in Enable OFF between two channel outputs. The delay between the two channels is 0.1 ms typical.

APPLICATION NOTES

Configuration Setting (CFG)

The configuration pin (CFG) sets several module configuration settings allowing the module to be used in applications without the need for loading configuration files. The settings are shown in Table 6. This must be done in order for the 2 modules to be recognized as part of a current sharing group.

Table 6. Configuration Setting Reference

RCFG (Kohm)	Fault Response	Diode Emulation	Current Limit (A)
6.98	Latch	Off	35
8.45/Open	Latch	Off	55
10.0	Latch	Off	70
11.5	Latch	Off	85

Table 7. Current Limits

CFG Current Limit (A)	35	55	70	85
IOUT_OC_FAULT_LIMIT	35	55	70	85
IOUT_AVG_OC_FAULT_LIMIT	24	40	52	64
IOUT_OC_WARN_LIMIT	21	35	47	59
IOUT_AVG_UC_FAULT_LIMIT	-24	-40	-52	-64
IOUT_UC_FAULT_LIMIT	-30	-50	-65	-80

APPLICATION NOTES

Charge Mode Control (ASCR) Setting (ASCRCFG)

The module's Charge Mode response can be optimized by adjusting the ASCR gain and residual settings, either by using the ASCRCFG pin-strap resistor method as shown in Table 8, or by using ASCR_CONFIG (DFh). When using Table 8, the ASCR Residual is fixed at 90, and the ASCR integral gain is fixed at 50.

Table 8. ASCRCFG Pin-Strap Settings

RASCRCFG (Kohm)	ASCR Gain	Clock Sync
6.98	250	Internal and Output Internal Clock
8.45	300	Internal and Output Internal Clock
10.0/Open	400	Internal and Output Internal Clock
11.5	500	Internal and Output Internal Clock
13.3	600	Internal and Output Internal Clock
15.4	700	Internal and Output Internal Clock
17.8	800	Internal and Output Internal Clock
20.5	1000	Internal and Output Internal Clock
23.7	250	External Clock
27.4	300	External Clock
31.6	400	External Clock
36.5	500	External Clock
42.2	600	External Clock
48.7	700	External Clock
56.2	800	External Clock
64.9	1000	External Clock

Note: ASCR gain must be set to the same value of each phase at multi-phase application.

APPLICATION NOTES

Multi-Phase Commands Setting

Extra commands are required for multi-phase application.

Table 9: Examples for 1 Module Commands Setting

1 Module (1+1 Configuration)		
Command Name	Master Phase (V_O2)	Satellite Phase (V_O1)
USER_CONFIG	0x1015	0x1016
INTERLEAVE	0x0000	0x0008
DDC_CONFIG	0x0200	0x0100
DDC_GROUP	0x00000000	0x00000000

1 Module (2 Phase 1 Output Configuration)		
Command Name	Master Phase (Phase 2)	Satellite Phase (Phase 1)
USER_CONFIG	0x1015	0x1016
INTERLEAVE	0x0000	0x0008
DDC_CONFIG	0x0101	0x2101
DDC_GROUP	0x00202020	0x00202020

Table 10: Examples for 2 Modules Commands Setting

2 Modules (1+3 Configuration)				
Command Name	Master Phase of V_O2	V_O1	Satellite Phase 1 of Vo2	Satellite Phase 2 of Vo2
USER_CONFIG	0x1015	0x1016	0x1016	0x1016
INTERLEAVE	0x0000	0x0008	0x0004	0x000C
DDC_CONFIG	0x0202	0x0100	0x2202	0x4202
DDC_GROUP	0x00202020	0x00000000	0x00202020	0x00202020

2 Modules (4 Phase 1 Output Configuration)				
Command Name	Master Phase	Satellite Phase 1	Satellite Phase 2	Satellite Phase 3
USER_CONFIG	0x1015	0x1016	0x1016	0x1016
INTERLEAVE	0x0000	0x0008	0x0004	0x000C
DDC_CONFIG	0x0103	0x2103	0x4103	0x6103
DDC_GROUP	0x00202020	0x00202020	0x00202020	0x00202020

Table 11: Examples for 3 Modules Commands Setting

3 Modules (3+3 Configuration)						
Command Name	Master Phase of V_O2	Satellite Phase 1 of V_O2	Satellite Phase 2 of V_O2	V_O1 Phase 1	Satellite Phase 1 of V_O1	Satellite Phase 2 of V_O1
USER_CONFIG	0x1015	0x1016	0x1016	0x1016	0x1016	0x1016
INTERLEAVE	0x0000	0x0006	0x000E	0x0008	0x0003	0x000B
DDC_CONFIG	0x0202	0x2202	0x4202	0x0102	0x2102	0x4102
DDC_GROUP	0x00202020	0x00202020	0x00202020	0x00202020	0x00202020	0x00202020
3 Modules (6 Phase 1 Output Configuration)						
Command Name	Master Phase	Satellite Phase 1	Satellite Phase 2	Satellite Phase 3	Satellite Phase 4	Satellite Phase 5
USER_CONFIG	0x1015	0x1016	0x1016	0x1016	0x1016	0x1016
INTERLEAVE	0x0000	0x0008	0x0003	0x000B	0x0006	0x000E
DDC_CONFIG	0x0105	0x2105	0x4105	0x6105	0x8105	0xA105
DDC_GROUP	0x00202020	0x00202020	0x00202020	0x00202020	0x00202020	0x00202020

APPLICATION NOTES

Table 12: Examples for 4 Modules Commands Setting								
4 Modules (3+5 Configuration)								
Command Name	Master Phase of Vo2	Vo1 Phase 1	Satellite Phase 1 of Vo1	Satellite Phase 2 of Vo1	Satellite Phase 1 of Vo2	Satellite Phase 2 of Vo2	Satellite Phase 3 of Vo2	Satellite Phase 4 of Vo2
USER_CONFIG	0x1015	0x1016	0x1016	0x1016	0x1016	0x1016	0x1016	0x1016
INTERLEAVE	0x0000	0x0008	0x0002	0x000A	0x0004	0x000C	0x0006	0x000E
DDC_CONFIG	0x0204	0x0102	0x2102	0x4102	0x2204	0x4204	0x6204	0x8204
DDC_GROUP	0x00202020	0x00202020	0x00202020	0x00202020	0x00202020	0x00202020	0x00202020	0x00202020
4 Modules (8 Phase 1 Output Configuration)								
Command Name	Master Phase	Satellite Phase 1	Satellite Phase 2	Satellite Phase 3	Satellite Phase 4	Satellite Phase 5	Satellite Phase 6	Satellite Phase 7
USER_CONFIG	0x1015	0x1016	0x1016	0x1016	0x1016	0x1016	0x1016	0x1016
INTERLEAVE	0x0000	0x0008	0x0002	0x000A	0x0004	0x000C	0x0006	0x000E
DDC_CONFIG	0x0107	0x2107	0x4107	0x6107	0x8107	0xA107	0xC107	0xE107
DDC_GROUP	0x00202020	0x00202020	0x00202020	0x00202020	0x00202020	0x00202020	0x00202020	0x00202020

APPLICATION NOTES

Surface Mount Information

Pick and Place

The LGA110D is designed with certain features to ensure it is compatible with standard pick and place equipment.
The low mass of typically 11.4 grams is within the capability of standard pick and place equipment. The choice of nozzle size and style and placement speed may need to be optimized.

The inductor has a flat area of 133.2 mm^2 (0.206 in^2) that can be used as a pick-up area.

PC Board Assembly Side

LGA110D module is not recommended for assembly on the bottom side of a customer board. If such an assembly is attempted, components may fall off the module during the second reflow process.

Moisture Sensitivity Level (MSL)

This module is classified as MSL level 3

Storage and Handling

The recommended storage environment and handling procedures for moisture-sensitive surface mount packages is detailed in J-STD-033 (Handling, Packing, Shipping and Use of Moisture/Reflow Sensitive Surface Mount Devices). Moisture barrier bags (MBB) with desiccant are required for MSL ratings of 2 or greater. These sealed packages should not be broken until time of use. Once the original package is broken, the floor life of the product at conditions of <= 30^{O}C and 60% relative humidity varies according to the MSL rating (See J-STD-033). The shelf life for dry packed SMT packages will be a minimum of 12 months from the bag seal date, when stored at the following conditions: < 40^{O}C, < 90% relative humidity.

Post Soldering Cleaning

Post solder cleaning is not recommended because it may affect the reliability of module.

APPLICATION NOTES

Pb-free Reflow Profile

This module will comply with IPC/JEDEC J-STD-020 (Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices) for both Pb-free solder profiles and MSL classification procedures. The standard provides reflow profile based on the volume and thickness of the module. The suggested Pb-free solder paste is Sn/Ag/Cu (SAC305). The recommended reflow temperature profile using SAC305 solder is shown below.

Tin-Pb Reflow Profile

The power modules are lead free modules and can be soldered either in a lead-free solder process or in a conventional Tin/Lead (Sn/Pb) process. It is recommended that the customer review datasheets in order to customize the solder reflow profile for each load board assembly. The following instructions must be observed when soldering these units. Failure to observe there instructions may result in the failure of or cause damage to the modules, and can adversely affect long-term reliability.

In a conventional Tin/Lead (Sn/Pb) solder process, peak reflow temperatures are limited to less than 235°C. Typically, the eutectic solder melts at 183°C, wets the land, and subsequently wicks the device connection. Sufficient time must be allowed to fuse the plating on the connection ensure a reliable solder joint. There are several types of SMT reflow technologies currently used in the industry. These surface mount power modules can be reliably soldered using natural forced convection, IR (radiant infrared), or a combination of convection/IR. For reliable soldering the solder reflow profile should be established by accurately measuring the modules block pin temperatures.

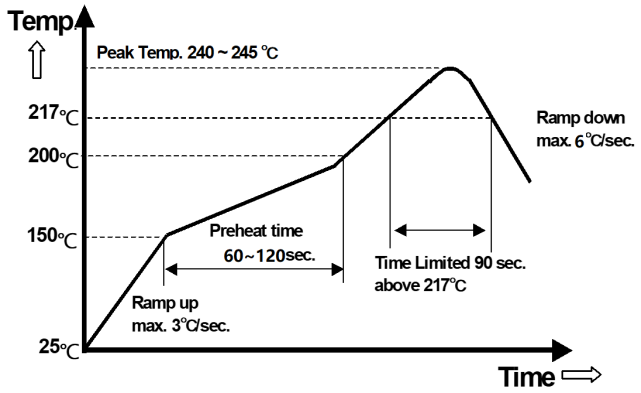


Figure 53 Recommended reflow profile using SAC305 solder paste

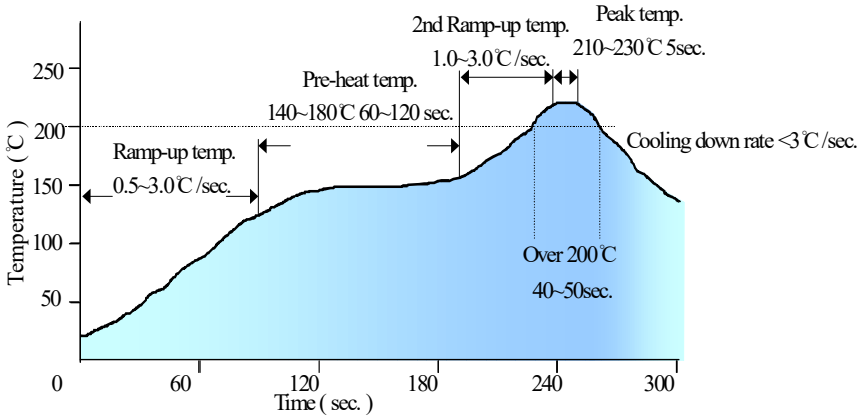


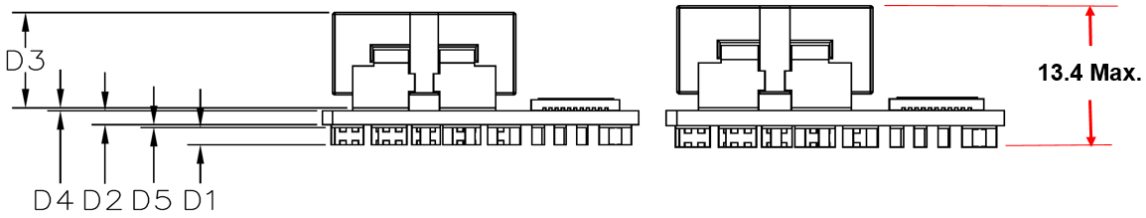
Figure 54 Recommended reflow profile

Note: 1. The stencil thickness for soldering module to load board is recommended as 5mil.
2. Recommended soldering Nitrogen process.

APPLICATION NOTES

Module Dimensions after Mounting

The following data shows the analysis height-tolerance that is expected for the LGA110D-01DADJJ module after it has been mounted to the host application PCB.



Ref	Description	Design Data Feature Type	Feature Dimension	
D1	Block PIN thickness	Machined	1.60	+0.04
				-0.04
D2	PCB thickness	Other	1.20	+0.12
				-0.12
D3	Inductor per max.height	Catalogue Size	10.3	+0.00
				-0.00
D4	Max solder paste thk (inductor)	Other	0.0243	+0.0193
				-0.0193
D5	Max solder paste thk (Block pin)	Other	0.03	+0.00
				-0.00

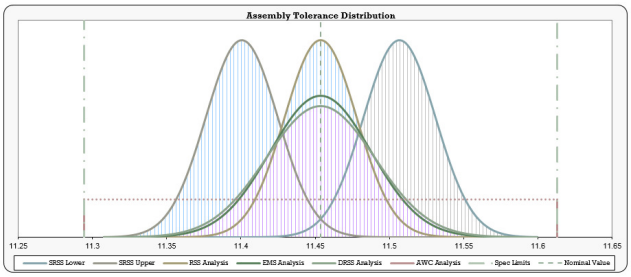
Arithmetic Worst Case (AWC) Analysis

Use for safety critical dimensions

Arithmetic Worst Case Analysis assumes all tolerances are at their worst extreme and that all out of specification parts have been removed through inspection.

Note: the nominal dimension is in the positive sense.

Nominal Dimension		Expected Value		Limit Values	Spec Parts All pass
13.1543	+0.1793	13.1542	+0.1793	13.3336 12.975	Yes
	-0.1793		-0.1793		



Height: Nominal = 13.1543 + 0.06 (solder thk on system board) = 13.2143 mm

Maximum = 13.3336 + 0.06 (solder thk on system board) = 13.3936 mm

Minimum = 12.975 + 0.06 (solder thk on system board) = 13.035 mm

RECORD OF REVISION AND CHANGES

Issue	Date	Description	Originators
1.0	09.06.2021	First Issue	C. Liu
1.1	11.08.2021	Update mechanical drawing	C. Liu
1.2	04.06.2022	Add patent information at the first page	C. Liu

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